

# International Technology Roadmap for Photovoltaic (ITRPV)

2017 Results



Ninth Edition, March 2018

In Cooperation with



Photovoltaik Equipment

# **International Technology Roadmap for Photovoltaic (ITRPV)**

**Results 2017**

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# 1. Executive summary

The photovoltaic (PV) industry needs to provide power generation products that can compete with both conventional energy sources and other renewable sources of energy. An international technology roadmap can help to identify trends and to define requirements for any necessary improvements. The aim of the International Technology Roadmap for Photovoltaic (ITRPV) is to inform suppliers and customers about anticipated technology trends in the field of crystalline silicon (c-Si) photovoltaics and to stimulate discussion on required improvements and standards. The objective of the roadmap is not to recommend detailed technical solutions for identified areas in need of improvement, but instead to emphasize to the PV community the need for improvement and to encourage the development of comprehensive solutions. The present, ninth edition of the ITRPV was jointly prepared by 55 leading international poly-Si producers, wafer suppliers, c-Si solar cell manufacturers, module manufacturers, PV equipment suppliers, and production material providers, as well as PV research institutes and consultants. The present publication covers the entire c-Si PV value chain from crystallization, wafering, and cell manufacturing to module manufacturing and PV systems. Significant parameters set out in earlier editions are reviewed along with several new ones, and discussions about emerging trends in the PV industry are reported.

The global PV module production capacity at the end of 2017 is assumed to be >130 GWp based on the 2016 data and a utilization of >80% [1, 2]; the market share of above 90% for the c-Si market and below 10% for thin-film technologies is unchanged [1]. This roadmap describes developments and trends for the c-Si based photovoltaic technology.

The PV module market increased significantly in 2017 while in parallel the module price reduction continued, but much slower than during 2016.

The implementation of advanced cell technologies and the use of improved materials resulted in higher average module power. The PV manufacturers increased their production capacities and continued cost reduction and the implementation of measures to increase cell efficiency. The price experience curve continued with its historic learning with a slight increase to about 22.8%. The PV industry could keep this learning rate up over the next few years by linking cost reduction measures with the implementation of enhanced cell concepts with improved Si-wafers, improved cell front and rear sides, refined layouts, and improved module technologies. This aspect is again discussed in this revision of the ITRPV. Improvements in these areas will result in 60 cell modules with an average output power of about 325 Wp for mc-Si and about 345 Wp p-type mono-Si respectively by 2028. 72 cell modules are expected to reach 390 Wp with mc-Si and 415 Wp for p-type mono Si respectively at that time. The combination of reduced manufacturing costs and increased cell and module performance will support the reduction of PV system costs and thus ensure the long-term competitiveness of PV power generation.

Roadmap activity continues in cooperation with VDMA, and updated information will be published annually to ensure comprehensive communication between manufacturers and suppliers throughout the value chain. More information is available at [www.itrpv.net](http://www.itrpv.net).

## 2. Approach

All topics throughout the value chain are divided into three areas: materials, processes, and products. Data was collected from the participating companies and processed anonymously by VDMA. The participating companies jointly agreed, that the results are reported in this roadmap publication. All plotted data points of the parameters reported are median values generated from the input data. As stated above, the topics are split into three areas: materials, processes, and products. Here, we address issues linked to crystallization, wafers, cells, modules, and PV systems for each of these areas respectively.

### 2.1. Materials

The requirements and trends concerning raw materials and consumables used within the value chain are described in this section. Reducing the consumption or replacing of some materials will be necessary in order to ensure availability, avoid environmental risks, reduce costs, and increase efficiency. Price development plays a major role in making PV-generated electricity competitive with other renewable and fossil sources of energy.

### 2.2. Processes

New technologies and materials, and highly productive manufacturing equipment, are required to reduce production costs. By providing information on key production figures, as well as details about processes designed to increase cell efficiency and module power output, this roadmap constitutes a guide to new developments and aims to support their progress. The section on processes identifies manufacturing and technology issues for each segment of the value chain. Manufacturing topics center on raising productivity, while technological developments aim to ensure higher cell and module efficiencies.

### 2.3. Products

Each part of the value chain has a final product. The product section therefore discusses the anticipated development of key elements such as ingots, wafers, c-Si solar cells, -modules and PV systems over the coming years.

## 3. PV learning curve

It is obvious that cost reductions in PV production processes should also result in price reductions [3]. Fig. 1 shows the price experience curve for PV modules, displaying the average module sales prices - at the end of the corresponding time period - (in 2017 US\$/Wp) as a function of cumulative module shipments from 1976 to 12/2017 (in MWp) [1, 2, 4, 5, 6]. Displayed on a log-log scale, the plot changes to an approximately linear line until the shipment value of 3.1 GWp (shipments at the end of 2003), despite bends at around 100 MWp. This indicates that for every doubling of cumulative PV module shipments, the average selling price decreases according to the learning rate (LR). Considering all data points from 1976 until 2017 we found an LR of about 22.8% - a slight increase compared to the 22.5% in the 8<sup>th</sup> edition. The large deviations from this LR plot in Fig.1 are caused by tremendous market fluctuations between 2003 and 2016.

The last two data points indicate the module shipment volumes in 2016, and 2017. For 2016 we assumed 76 GWp (2016 PV installation data in [1]). The 2017 value is calculated to 105 GWp: the average installation of 2017 as assumed in [7-9] is calculated to be 99 GWp, for shipments we have added 6 GWp shipped to US warehouses until the end of 2017 in preparation of the “Suniva trade case” [10]. The corresponding module prices at the end of 2016 and 2017 are 0.37 US\$/Wp and 0.34 US\$/Wp respectively [6]. Based on this data the cumulated shipped module power is calculated to be approximately 414 GWp. The calculated worldwide installed module power reached 402 GWp end of 2017 after 303 GWp in 2016 [1].

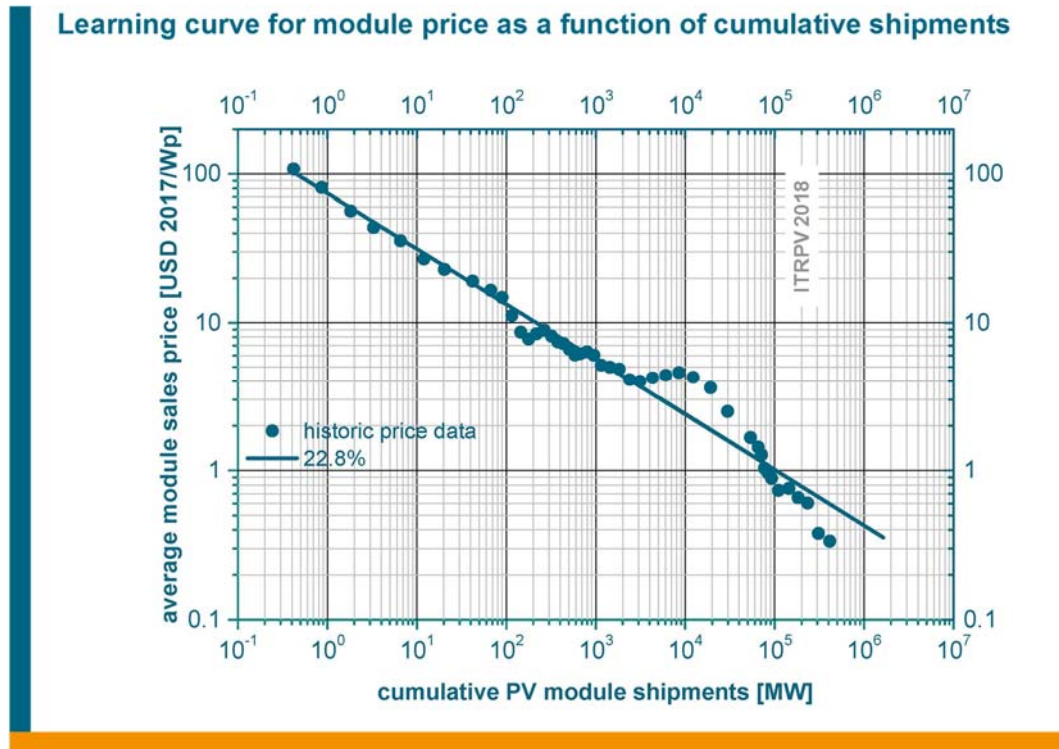
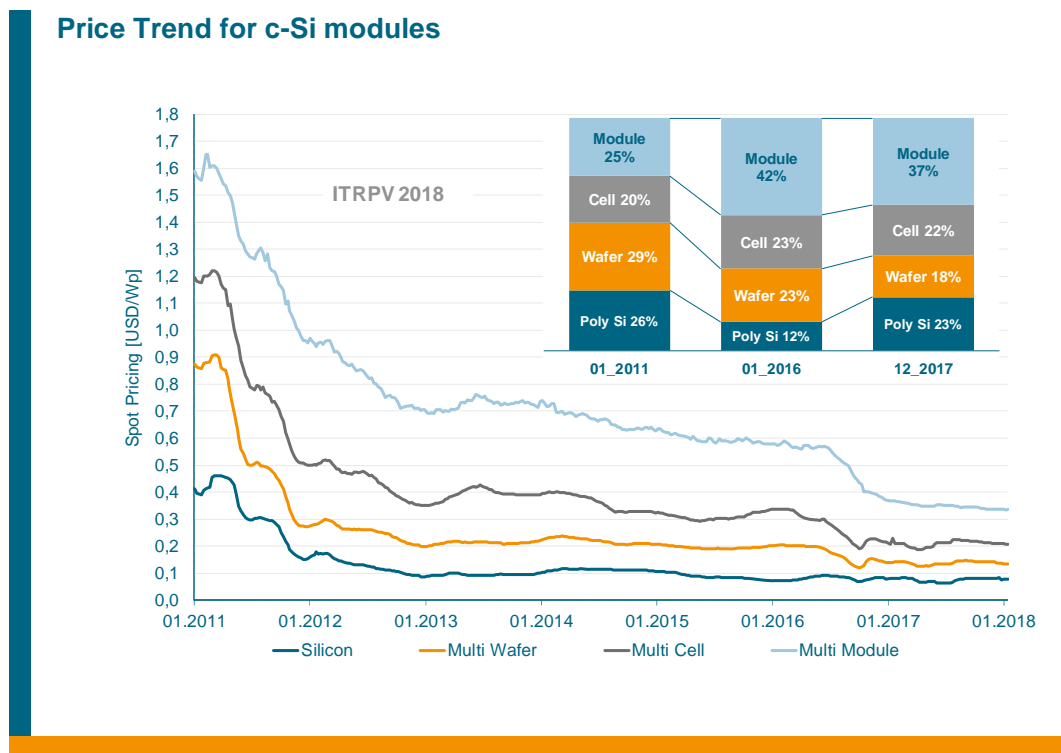


Fig. 1: Learning curve for module price as a function of cumulative PV module shipments.

## 4. Cost consideration

Fig. 2 shows the price development of mc-Si modules from January 2011 to January 2018 with separate price trends for poly-Si, multi crystalline (mc) wafers, and cells [6]. After the tremendous price erosion during the second half of 2016 we saw a quite smooth price decline during 2017. Module production capacity is assumed to be >130 GWp, exceeding cell production capacity of >110 GWp at the end of 2017 due to additional capacity expansions [1, 2]. If capacity expansion will continue in 2018 without a further market increase, a critical oversupply situation may occur. PV module self-consumption in China lowers the risk but the final market growth remains unpredictable [7, 9, 11]. The inset of Fig. 2 shows the comparison of the proportion of prices attributable to silicon, wafer, cell, and module price. The overall price level difference between 01/2016 to 12/2017 is about 40% but between 01/2017 and 12/2017 the decrease was only about 9% and the share of the different price elements remained nearly constant during 2017. The price fraction of poly-Si is at around 23%. Wafer and cell

conversion prices decreased, and module conversion remained at 37% during 2017.



**Fig. 2:** Price trends for poly-Si, mc-Si wafers, cells, and c-Si modules (assumption 12/2017: 4.2g poly-Si per Wp, average mc-Si cell efficiency of 18.85% {4.59Wp}); inset: comparison of the proportion of the price attributable to different module cost elements between 01/2011, 01/2016, and 12/2017 (1.60, 0.57, and 0.34 US\$/Wp) [6].

The non-silicon module manufacturing costs are mainly driven by consumables and materials as discussed in the c-Si PV module cost analysis in the 3rd edition of the ITRPV. Taken into account the fact that the anticipated global PV module production capacity of about 130 GWp in 2017 will further increase in 2018 due to continued capacity expansions, the production capacity will again exceed the predicted global market demand of >100 GWp in 2018 [9, 11]. Therefore, prices will not compensate for any cost increases as there is no shortage expected — in other words, the pressure on wafer, cell and - more painful - on module manufacturing — will persist. Achieving cost reductions in consumables, and materials will be more difficult but have to be continued. Improving productivity and product performance will become even more important.

The known three strategies, emphasized in former ITRPV editions help to address this challenge:

- Continue the cost reduction per piece along the entire value chain by increasing the Overall Equipment Efficiency (OEE) of the installed production capacity and by using Si and non-Si materials more efficiently.
- Introduce specialized module products for different market applications (i.e. tradeoff between cost-optimized, highest volume products and higher price fully customized niche products).
- Improve module power/cell efficiency without significantly increasing processing costs.



The latter implies that efficiency improvements need to be implemented with lean processes that require minimum investment in new tool sets, including the extension of the service life of depreciated tool sets in order to avoid a significant increase in depreciation costs.

It will remain difficult to introduce new, immature technologies that do not show reductions of the cost per Wp from the beginning.

## 5. Results of 2017

### 5.1. Materials

#### 5.1.1. Materials – crystallization and wafering

With around 23% share poly-Si remains the most expensive material of a c-Si module as discussed in 4. The Siemens and the FBR (Fluidized Bed Reactor) processes remain the main technologies for the production of poly-Si. Fig. 3 shows that Siemens process will stay the mainstream technology during the next 10 years. As FBR processing is consuming less electricity it is assumed that its share will increase against Siemens processing. Other technologies such as umg-Si or direct wafering technologies are not expected to yield significant cost advantages compared to conventional poly-Si technologies over the coming years but are expected to be available in the market with a small market share between about 1% in 2017 to around 9% in 2028.

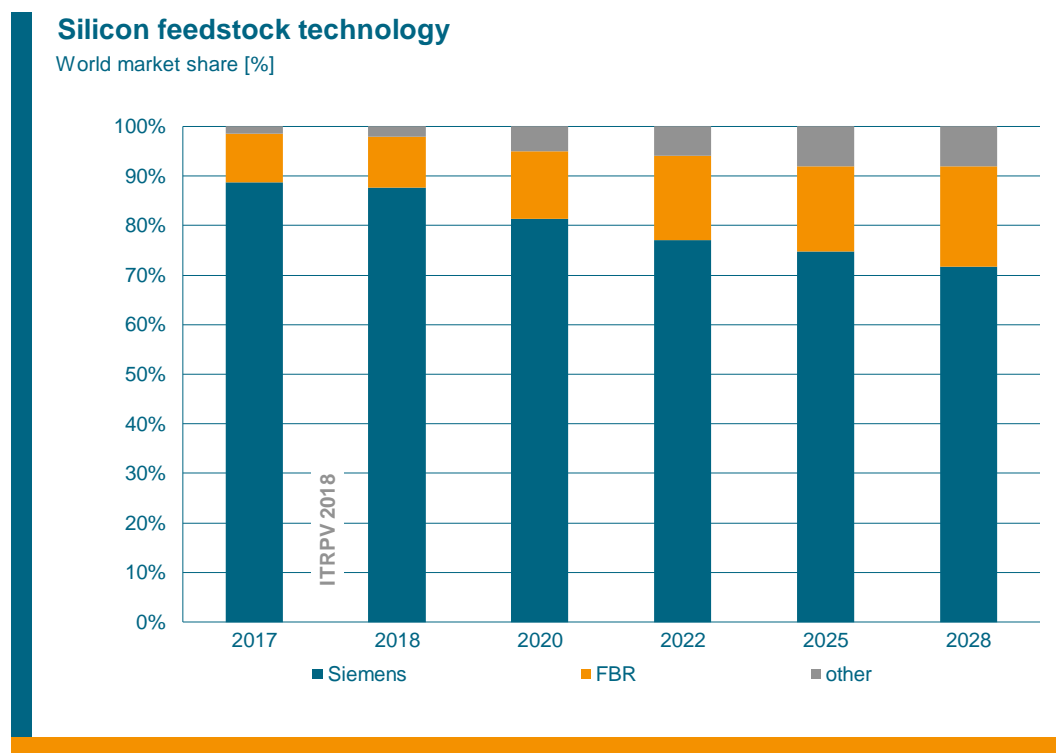


Fig. 3: Expected change in the market share of poly-Si production technologies.



The introduction of diamond wire sawing (DWS) has been a significant improvement in terms of wafering process cost reductions. DWS nearly completely replaced slurry-based wafer sawing for mono-Si as shown in Fig. 4.

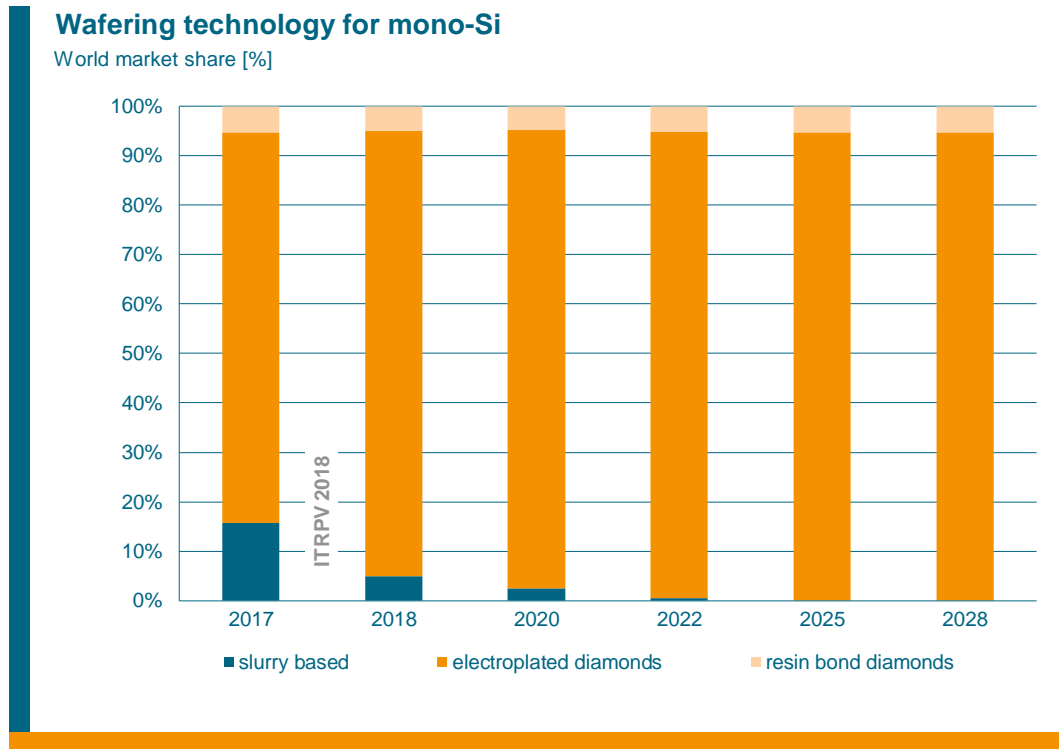


Fig.4: Market share of wafering technologies for mono-Si.

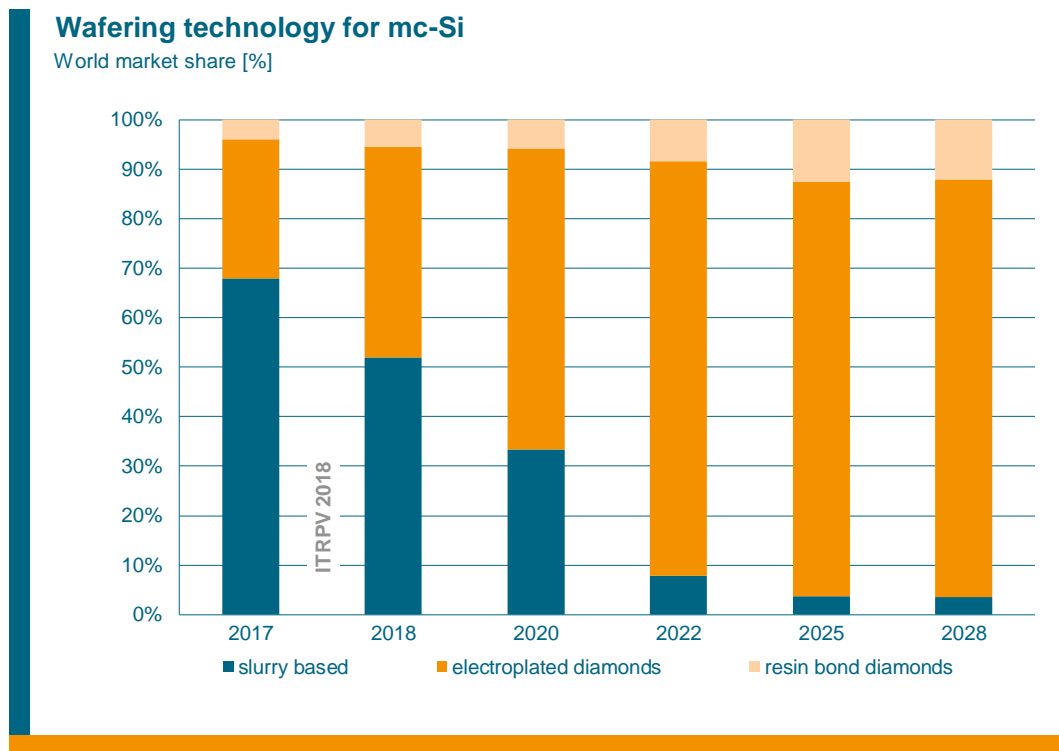


Fig. 5: Market share of wafering technologies for mc-Si.

Despite slurry-based wafering was still mainstream in mc-Si wafer sawing in 2017, it is expected to be very fast replaced by DWS technology with a market share of already greater than 50% in 2018 as shown in Fig. 5.

This change is supported by the fast introduction of wet chemical texturing methods for DWS mc-Si as will be discussed in 5.2.2. Electroplated diamond wire is considered as the dominating wire material. We do not believe that other new wafer manufacturing techniques, especially kerf less technologies, will gain significant market shares, mainly due to the maturity of the established sawing technologies.

Producing thinner wafers, reducing kerf loss, increasing recycling rates, and reducing the cost of consumables, can yield savings. Wire diameters will be reduced continuously over the next few years.

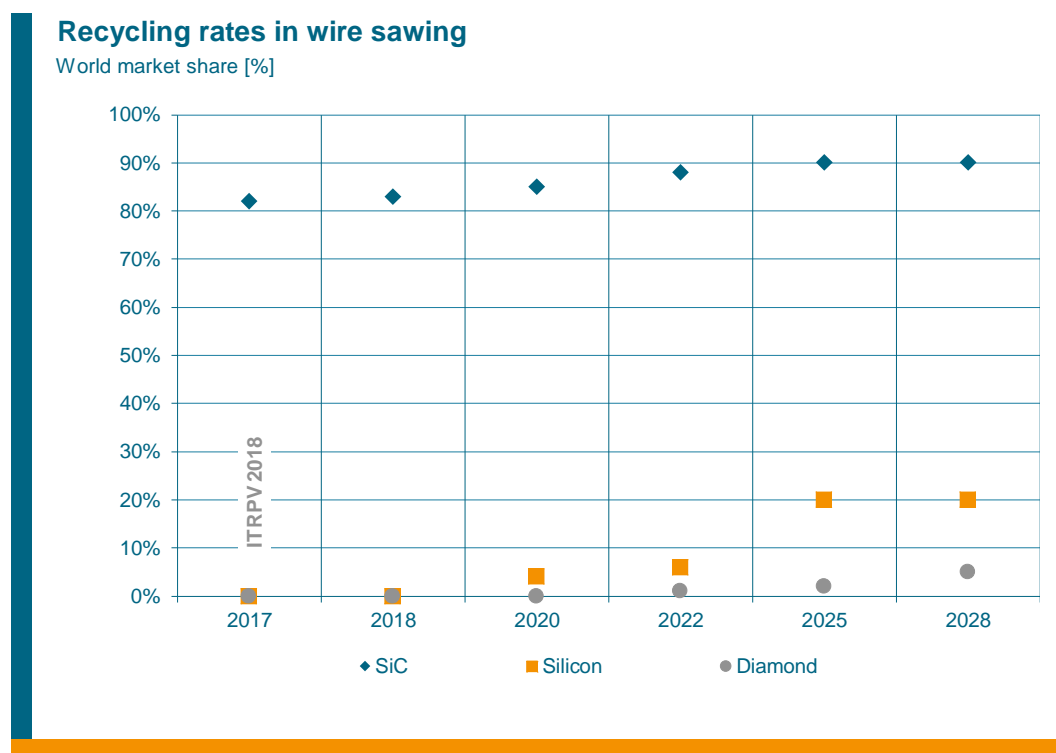


Fig. 6: Recycling rates of some consumables in wafering.

Fig. 6 shows the expected recycling rates of SiC, Diamond wire and Si. There will be more recycling of Si and diamond wire over the next years while SiC recycling rate is expected to increase only slightly from 80% to about 90% within the next 10 years.

DWS results in significant higher utilization of poly-Si as shown in Fig.7. About 15% less poly-Si is consumed per wafer in case of DWS. This is mainly caused by the reduced kerf loss as will be discussed in 5.2.1. The weight of a 180 $\mu$ m M2 mono-Si / 156.75 mm x 156.75 mm mc-Si wafer is about 10 g. Nearly twice as much poly-Si is consumed for one slurry based sawed wafer and still about 160% for a DWS wafer. This amount is expected to be significantly reduced over the next years.

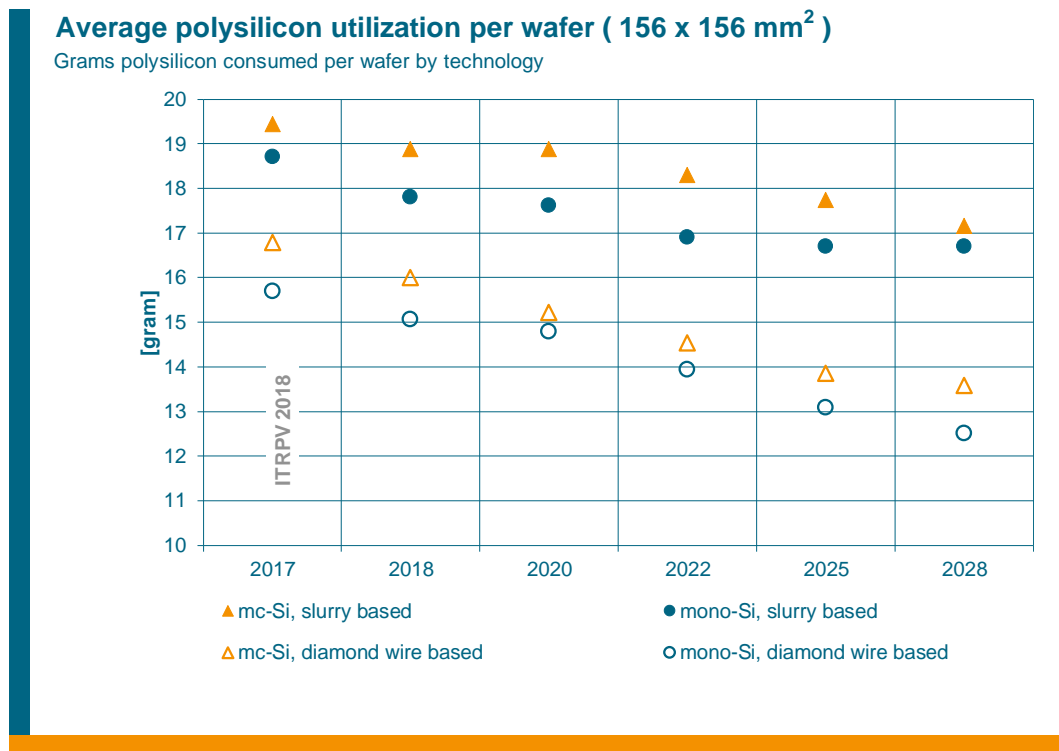


Fig. 7: Average poly-Si consumption for mc-Si and mono wafers with different wafer sawing technologies.

### 5.1.2. Materials – cell processing

Si wafers account for approximately 40% of today's cell price, as shown in Fig. 2. Reducing as-cut wafer thickness will lead to more efficient use of silicon. The developments anticipated in previous editions of the roadmap – also in the last edition - did not materialize due to a sufficient availability of poly-Si [1, 8]. A thickness of 180  $\mu\text{m}$  is still preferred for mc-Si and mono-Si wafers used in contemporary cell and module production lines as shown in Fig. 8, mainly due to the higher stability. 160  $\mu\text{m}$  mono wafers are already in mass production by today as discussed in the ITRPV's 8<sup>th</sup> edition. It is assumed that the thickness of mc-Si wafers will slowly approach a minimum value of 150  $\mu\text{m}$  until 2025. Mono-Si wafer thickness will follow a faster thickness reduction down to 130  $\mu\text{m}$  in 2028. Module technology is ready today for thicknesses down to 140  $\mu\text{m}$ .

Metallization pastes/inks containing silver (Ag) and aluminum (Al) are the most process-critical and most expensive non-silicon materials used in current c-Si cell technologies. Paste consumption therefore needs to be reduced. Fig. 9 shows our estimations regarding the future reduction of the silver that remains on a 156x156 mm<sup>2</sup> cell after processing. The reduction of remaining Silver per cell is expected to continue during the next years. The current study found 100 mg as the median value for 2017 and 90 mg for 2018 – slightly above the estimation in the 8<sup>th</sup> edition. A reduction down to 50 mg per cell is expected to be possible by 2028 – also more conservative than in last year's survey. New developments in pastes and screens will enable this reduction, and this clearly shows the reaction of suppliers to the needs of cell manufacturers. The average silver price of 533 US\$/kg middle of February 2018 [12] results in costs of 4.8 US\$ cents/cell (1 US\$ cents/Wp, for a 20% mc-Si PERC cell), or about 13% of the non-Si cell price, shown in Fig. 2.

### Trend for minimum as-cut wafer thickness and cell thickness

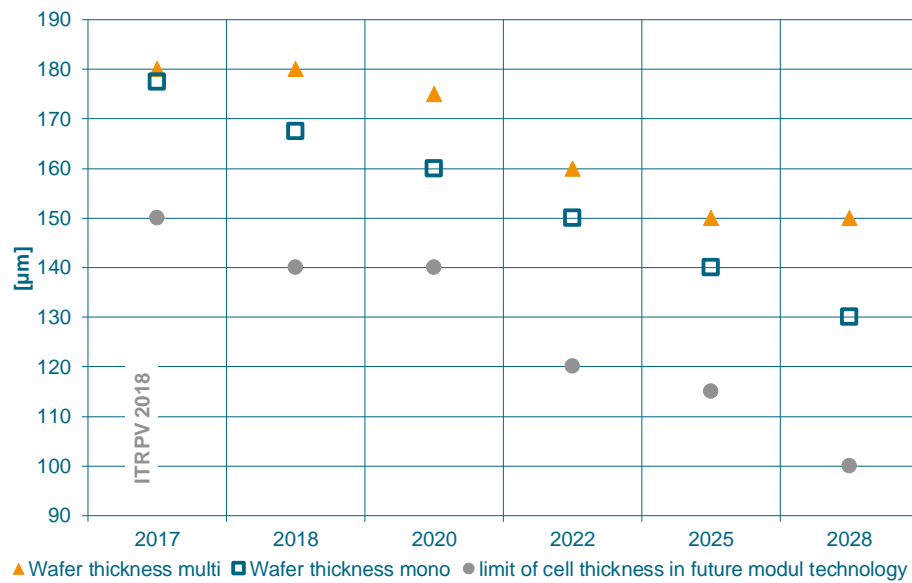


Fig. 8: Predicted trend for minimum as-cut wafer thickness and cell thickness for mass production of c-Si solar cells and modules.

Because silver will remain expensive due to the world market dependency, it is extremely important to continue all efforts to lower silver consumption as a means of achieving further cost reductions.

### Trend for remaining silver per cell (156x156mm<sup>2</sup>)

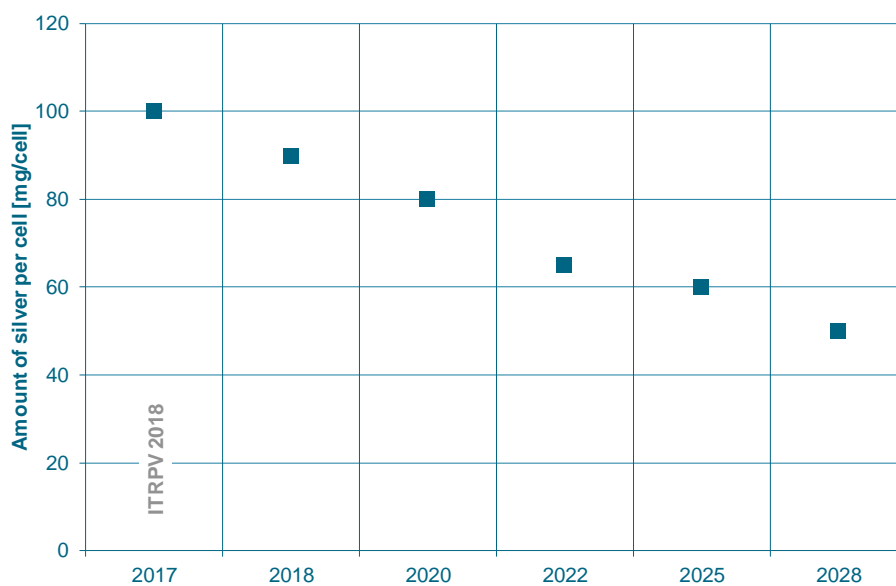


Fig. 9: Trend for remaining silver per cell (156 x 156 mm<sup>2</sup>).

Despite a continuous reduction of silver consumption at the cell manufacturing level, silver replacement is still considered as we will discuss in chapter 5.2.2. Copper (Cu), as less expensive material, applied with plating technologies, is the envisioned substitute. It is still assumed that it will be introduced in mass production, but the market share is considered more conservative than in the last edition with a market share of <15% in 2028 – a further delay versus former ITRPV expectations. Technical issues related to reliability and adhesion have to be resolved before alternative metallization techniques can be introduced. Appropriate equipment and processes also need to be made ready for mass production. Silver is expected to remain the most widely used front side metallization material for c-Si cells in the years to come.

Pastes containing lead are restricted in accordance with legislation that went into effect in 2011 under the EU Directive on the Restriction of Use of Hazardous Substances (RoHS 2). This restriction affects the use of lead and other substances in electric and electronic equipment (EEE) on the EU market. It also applies to components used in equipment that falls within the scope of the Directive. PV panels are excluded from RoHS 2, meaning that they may contain lead and do not have to comply with the maximum weight concentration thresholds set out in the directive<sup>1</sup>. PV's exclusion from the Directive will remain in effect for the next few years — a review of RoHS 2 will likely take place by mid-2021 at the latest<sup>2</sup>. Cell manufacturers should act carefully, especially, as the exclusion in question is limited to PV panels installed in a defined location for permanent use (i.e. power plants, rooftops, building integration etc.). Should the component in question also be useable in other equipment that is not excluded from RoHS 2 (e.g. to charge calculators), then the component must comply with the Directive's provisions.

We anticipate lead free pastes to become widely used in the mass production of c-Si cells in 2019/2020.

### 5.1.3. Materials – modules

Module add-on costs are clearly dominated by material costs. Improvements in module performance as shown in Section 5.3 and reductions in material costs are therefore required if module add-on costs should be reduced. Approaches for increasing performance include the reduction of optical losses (e.g. reflection of front cover glass) and the reduction of interconnector losses. Approaches for reducing material costs include:

- Reducing material volume, e.g. material thickness.
- Replacing (substituting) expensive materials.
- Reducing waste of material.

The most important material of a module is the front side glass. It mainly determines weight and light transmission properties. The thickness is also important regarding mechanical stability.

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<sup>1</sup> Article 2(i) of the RoHS Directive [2011/65/EU] excludes from the scope of the Directive “photovoltaic panels intended to be used in a system that is designed, assembled and installed by professionals for permanent use at a defined location to produce energy from solar light for public, commercial, industrial and residential applications.”

<sup>2</sup> Article 24 of the RoHS Directive [2011/65/EU] requires an evaluation and possible revision of the Directive, including its scope, by July 22, 2021.

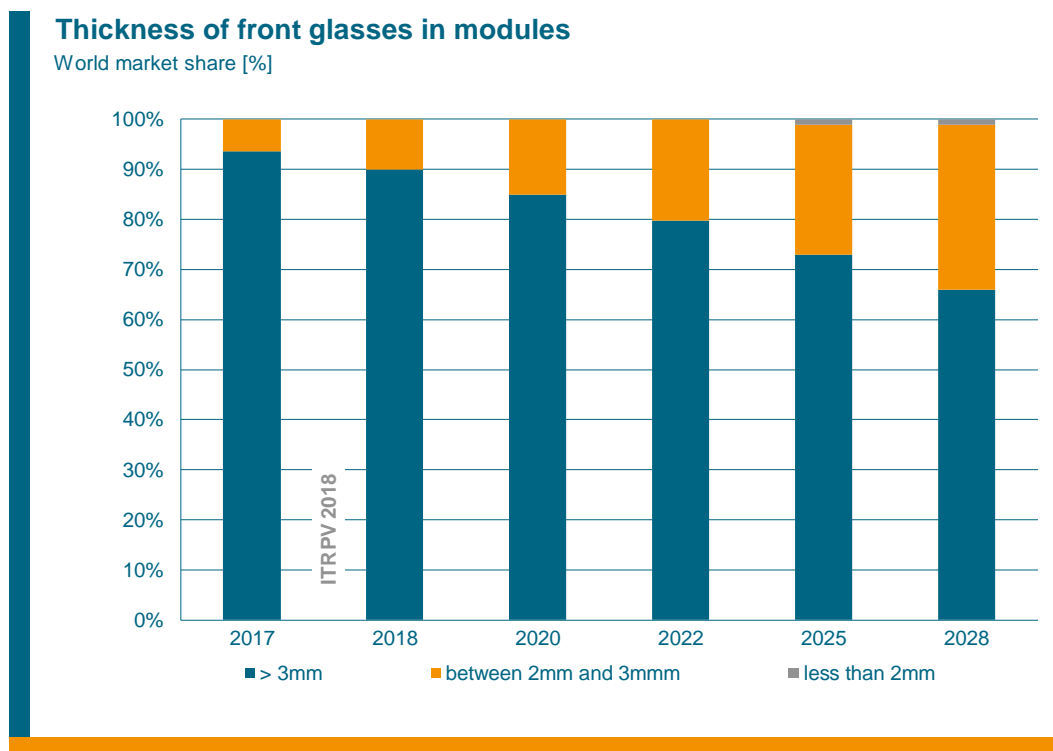


Fig. 10: Expected trend of front side glass for c-Si modules.

Fig. 10 summarizes the expected trend in front side glass thickness. It is expected that a reduction to between 3mm and 2mm thickness will appear over the next years. A thickness below 2mm is not expected to have significant market share.

The use of antireflective (AR) coatings has become common in recent years as a mean of improving the transmission of the front cover glass. AR-coated glass will remain the dominant front cover material for c-Si PV modules in the future, with market shares well above 90%.

Since AR-coated glass will be the most commonly used front cover, it is important that the AR coating remains effective and stable under various outdoor conditions during the entire lifecycle of the module. It appears that not all AR coatings on the market meet this requirement even for a 10-year period. However, there is a clear trend indicating that the average service life of these coatings will improve over the next seven years to a level in the range of the anticipated module service life as shown in Fig. 11.

### Expected lifetime of AR-coating on module front glass

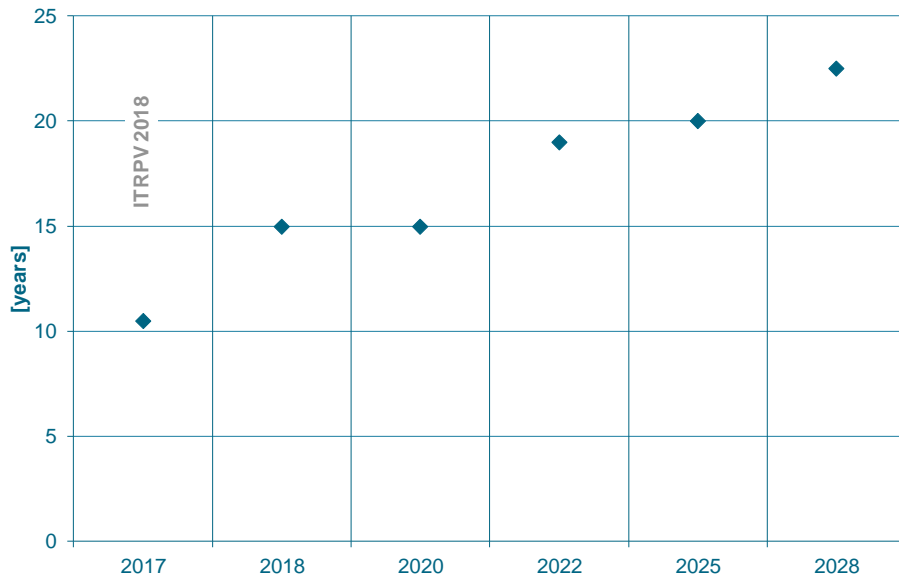


Fig. 11: Predicted trend for the average service life of AR coatings on front glass.

### Different technologies for cell interconnection

World market share [%]

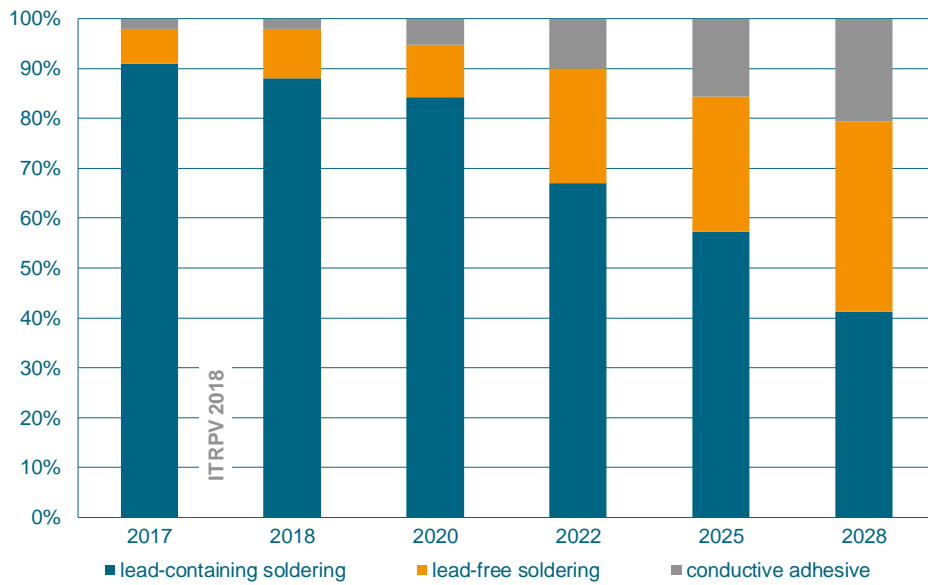


Fig. 12: Expected market shares for different cell interconnection technologies.



For a long period of time, solders that contain lead have served as the standard interconnection technology for solar cells in module manufacturing. Due to environmental and other considerations as discussed in chapter 5.1.2, more and more PV manufacturers are striving towards lead-free alternatives, as can be seen in Fig. 12.

Lead containing solders will stay mainstream during the next years, but lead-free solder and conductive adhesive technologies are expected to gain market shares over the next years. In the long-term perspective, these lead-free interconnection technologies are expected to advance to become the leading technologies.

With regard to the interconnector material, copper ribbons will remain the dominating material as shown in Fig. 13. Copper-wires are expected to gain over 30% market share during the next decade.

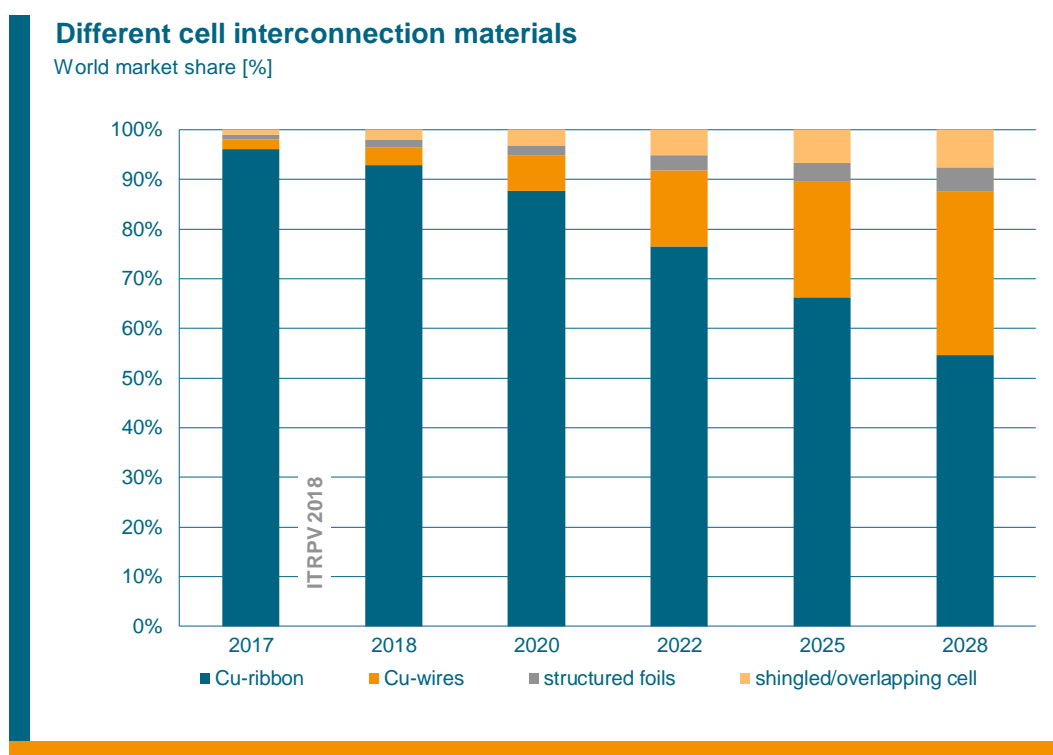


Fig. 13: Expected market shares for different cell interconnection materials.

Structured foils mainly used as an interconnection of back contact cells are expected to stay a niche technology with a market share of <3% while shingled or overlapping cell interconnection, as a 2<sup>nd</sup> niche technology might gain a market share of above 5% until 2028.

It is important to note that the up-and-coming interconnection technologies will need to be compatible with the ever-thinner wafers that will be used in the future. In this respect, low-temperature approaches using conductive adhesives or wire-based connections have an inherent advantage due to the lower thermal stresses associated with them.

Similar to the cell interconnection we find a clear trend towards lead-free module interconnection covering all interconnections between the cell strings and the junction box, as shown in Fig. 14. Conductive adhesives and lead-free interconnects are expected to become equal alternatives to lead containing technologies with increasing market shares.

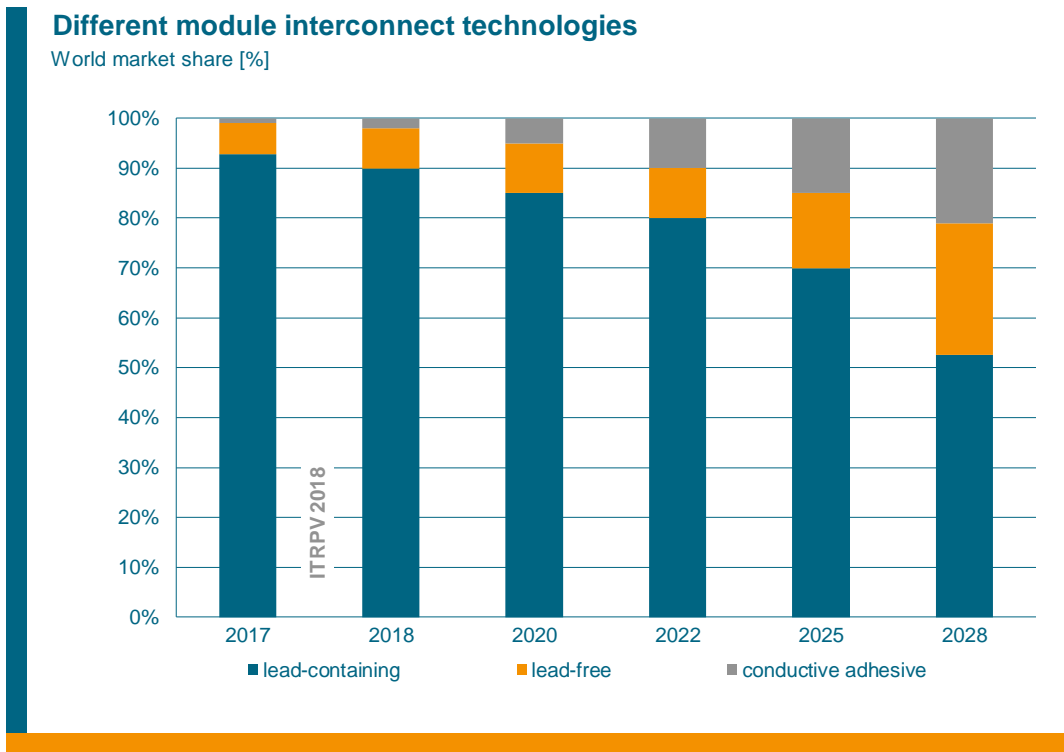


Fig. 14: Expected market share of different module interconnection material.

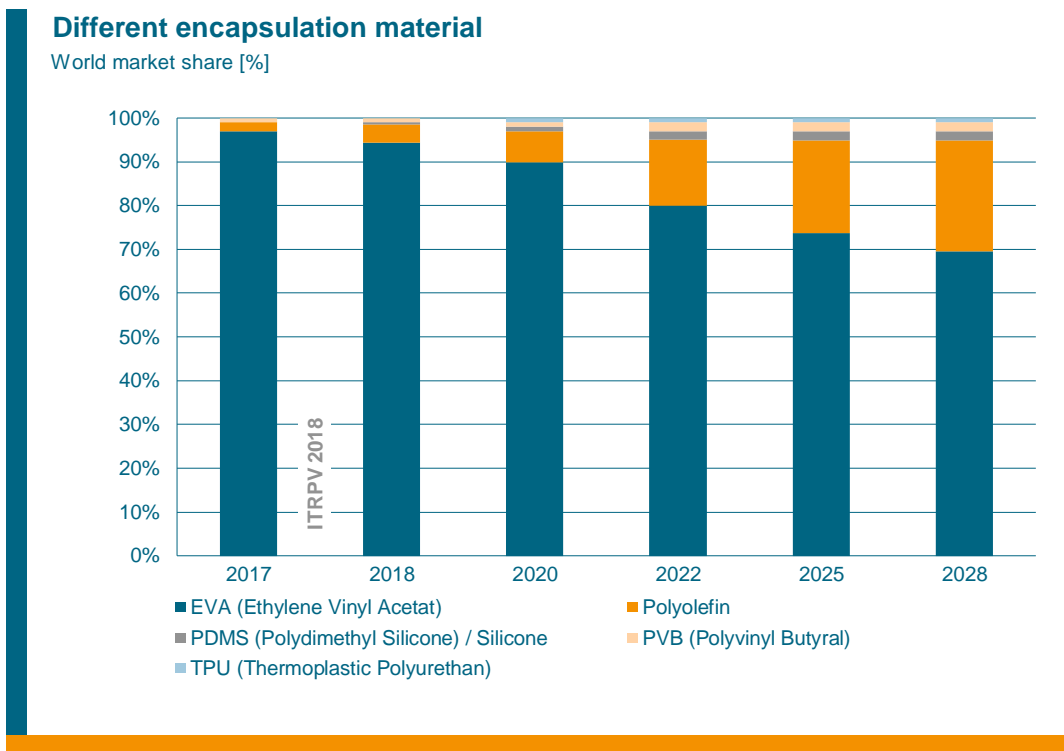
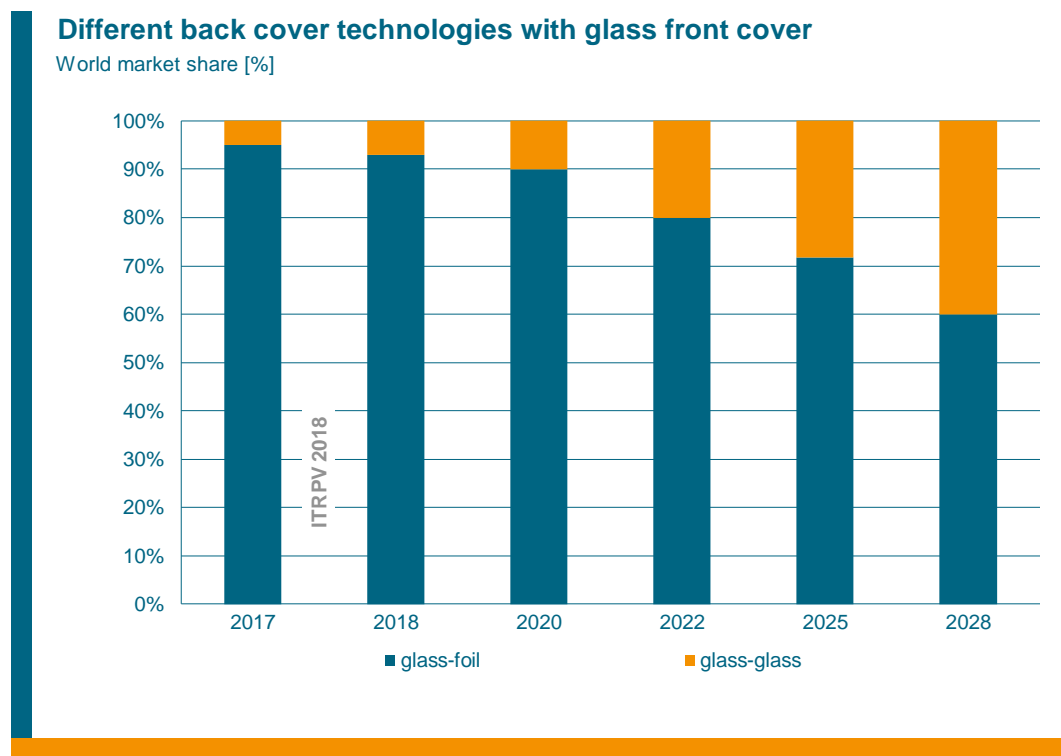


Fig. 15: Expected market shares for different encapsulation materials.

The encapsulation material and the back sheet are key module components. Both are also major cost contributors in module manufacturing. Intensive development efforts have been made to reduce the cost of these materials. At the same time maintaining or even improving the properties of this key

components is mandatory to ensure the module service life time. This has led to a trend toward new materials, as shown in Fig. 15 for encapsulation materials. However, it is also predicted that EVA will remain the dominant encapsulation material with a market share well above 60% over the ten-year period of this survey.

As can be seen in Fig. 16, foils will stay mainstream as back cover material, but glass is expected to gain a significant higher market share as backside cover material for c-Si modules over the next decade and increase its market share from 5% in 2017 to 40% in 2028.



**Fig. 16:** Share of glass-foil and glass-glass as back cover technologies.

The expected share of different back cover foils is summarized in Fig. 17. Tedlar based foils are expected to stay mainstream.

Fig. 18 looks at the trends for frame materials. Currently modules with aluminum frames are clearly dominating the market.

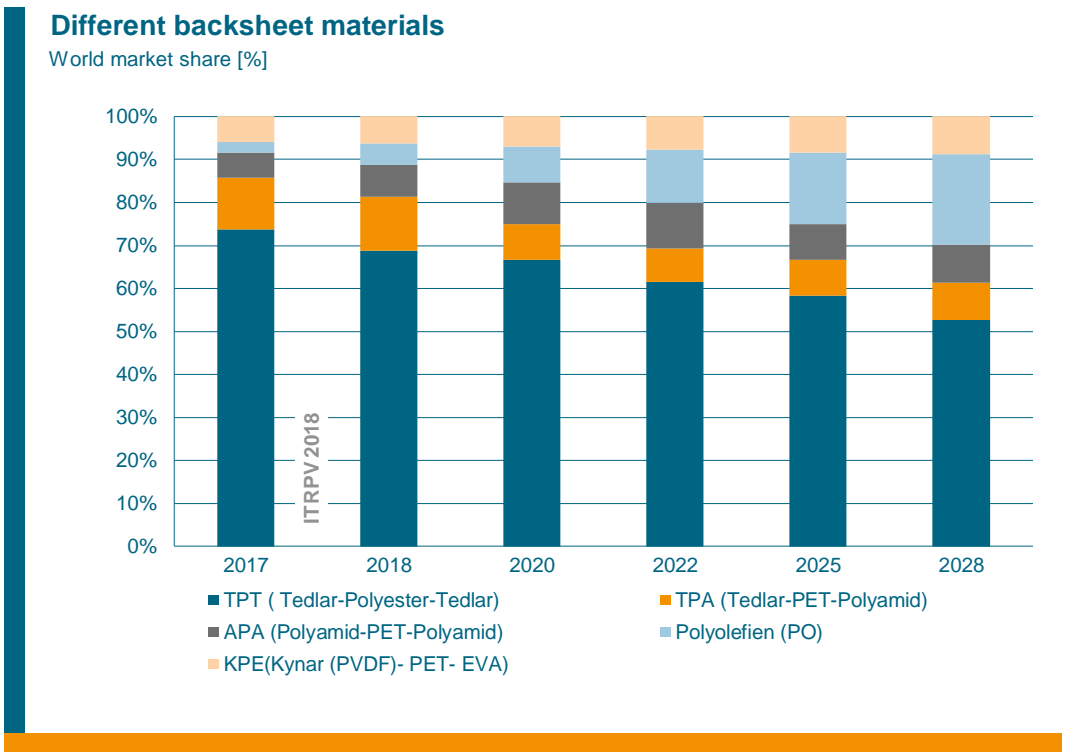


Fig. 17: Back cover foil materials.

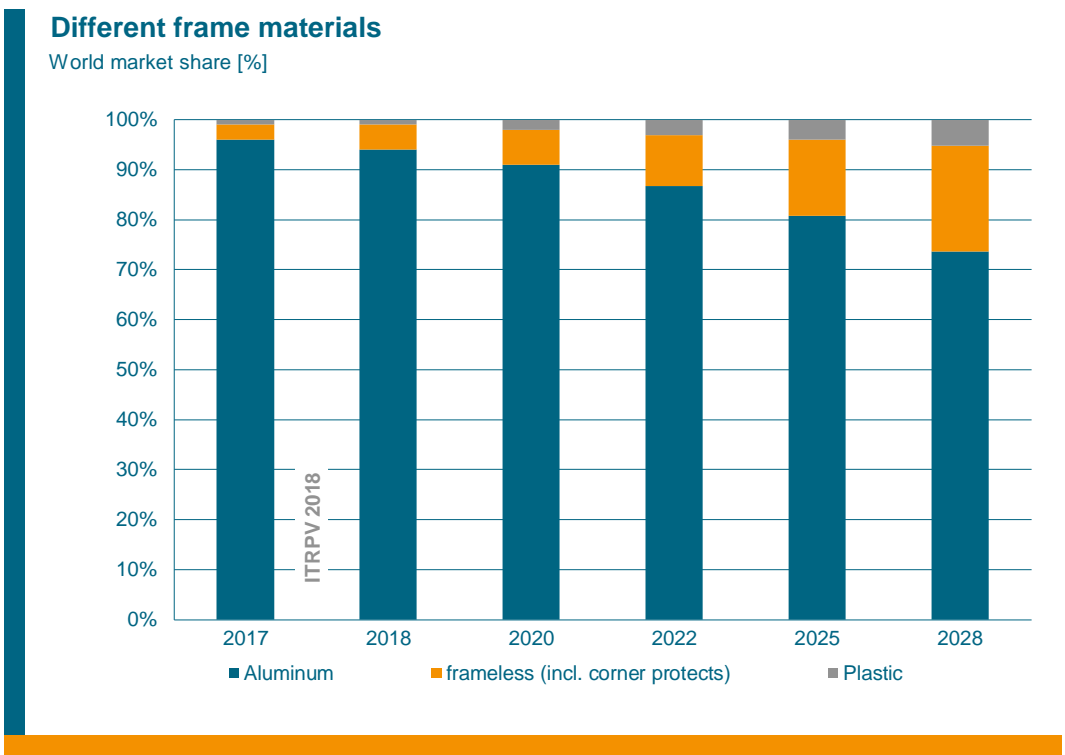


Fig. 18: Expected market shares for frame materials.

Frameless modules are expected to increase its market share to above 20% in 2028. Plastics frames are expected to enter slowly into the market while other materials are not expected to have market shares above 1% until 2028.

In order to maintain quality (for thinner cells as well), the solar cells used for module assembly should be free of micro cracks. The majority of the contributing companies are now testing all of their products during the manufacturing process. Among other things, the contributors have agreed to offer Potential Induced Degradation (PID)-resistant cell and module concepts only.

Over testing for PID is still common. Many test labs employ test conditions beyond the minimum levels described in IEC TS 62804. Currently IEC TC82 is working on a next edition of IEC 61215 which will likely include testing for PID. The test conditions are still under discussion. At the same time, there has been no industry-wide accepted and applied definition of micro-cracks.

## 5.2. Processes

### 5.2.1. Processes – manufacturing



Fig. 19: Predicted trend for ingot mass for mc-Si and for mono-Si.

It is possible to increase the throughput of the crystallization process by changing the common sizes of the ingots. Fig. 19 shows the increase in ingot mass for casted silicon materials and for Czochralski / Continuous Czochralski (Cz/CCz) growth of mono-Si, as predicted by the roadmap. Gen6 ingoting will be mainstream with ingot masses of 900 kg in 2018. Starting in 2019, the transition to Gen8 will start, may be with implementing a G7, by enabling ingoting with masses of up to 1,000 kg in 2020 mainstream. Casted ingot mass will increase further towards 1,200 kg and will mark the move to Gen8 after 2020. Transition to Gen8 in mass production may go even faster. The ingot mass of mono is expected to increase within the next 10 years but slower as expected in former ITRPV editions. CCz is expected to have only a small increase in market share over classical Cz. Float zone (FZ) material will not be used anymore for PV mass production.

Fig. 20 summarizes the anticipated throughput developments of crystal growth and wafering technologies. The throughput of crystal growth for both types, casted and mono, will be continuously increased by up to 30% for casting and up to 20% pullers over the next 10 years.

A similar trend is visible for wafering. Diamond wiring will increase the throughput by up to 30% within the next 10 years while slurry-based throughputs will stop further improvement within the next years.

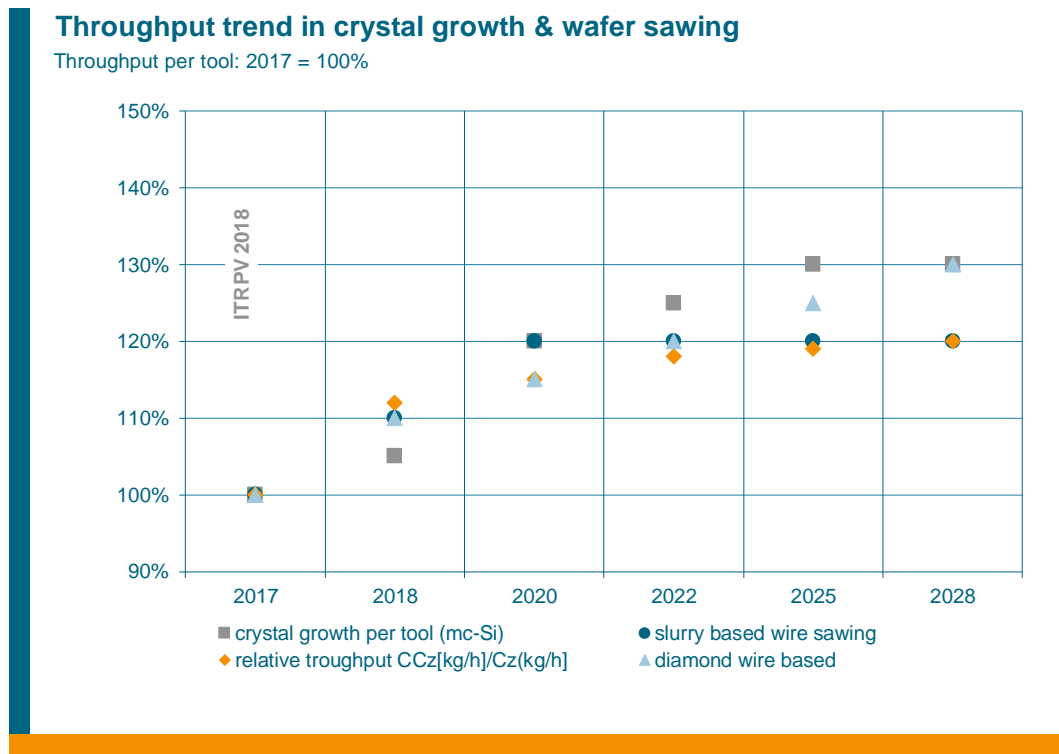


Fig. 20: Predicted trend for throughput per tool in crystal growth & wafer sawing technologies

Yield enhancement by reducing the kerf loss will further improve productivity in wafering on top of the effect of the increased throughput. This is important to improve the usage of poly-Si as discussed in 5.1.1.1. Fig. 21 describes the trend for kerf loss and for Total Thickness Variation (TTV). The kerf loss of slurry-based sawing is generally higher than for diamond wire-based sawing, not much progress is expected, mainly due to the shrinking market share. Today's kerf loss of about 125  $\mu\text{m}$  for slurry-based will stop at 120  $\mu\text{m}$ . A kerf width of 85  $\mu\text{m}$  is standard for diamond wire-based sawing. It is predicted to decline to 60  $\mu\text{m}$  until 2028. This underscores the long-term advantages of diamond wiring technology, one reason for the success of this technology as shown in Fig. 4 and Fig. 5. Today's TTV is 20  $\mu\text{m}$  for it is expected to stay constant in the future.

### Kerf loss and TTV for slurry based and diamond wire sawing

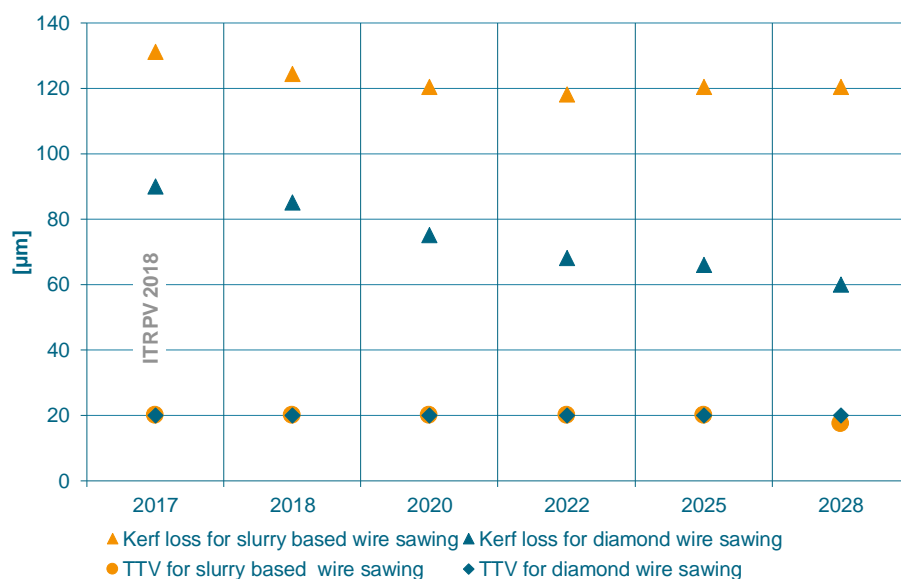


Fig. 21: Kerf loss and TTV.

### Conversion cost for wafer slicing and ingot growth

(2017 = 100%)

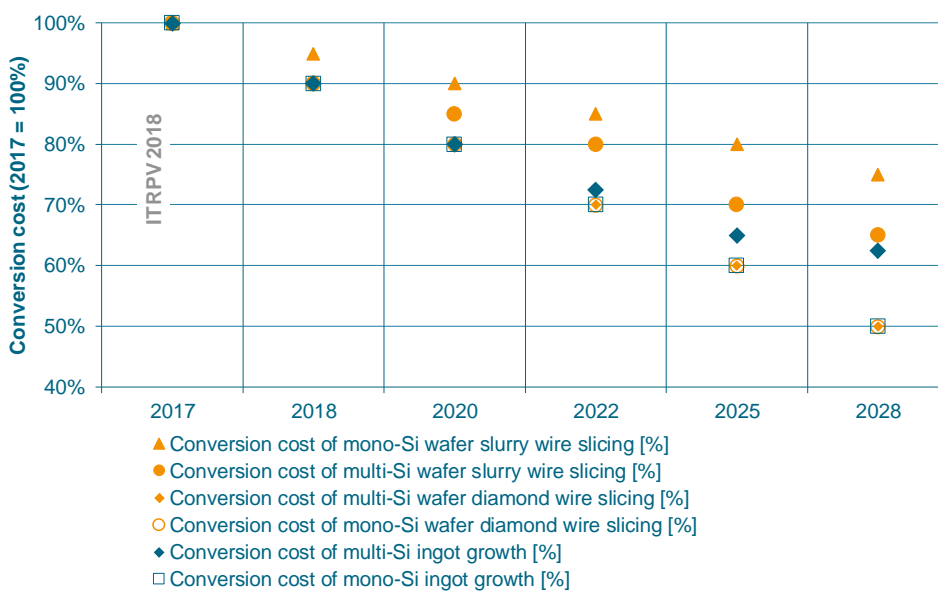


Fig. 22: Trend of conversion cost for crystallization and wafering technologies.

Fig 22 shows the resulting cost reduction trends for the discussed crystallization and wafering technologies. Mono crystal growth and mc-Si diamond wiring technology are expected to have the biggest



potential with halving the cost until 2028. Slurry based wafering will only show larger cost reduction in mc-Si wafering.

Optimizing productivity is essential to stay cost competitive. Increasing the throughput of the equipment in order to achieve maximum output is therefore a suitable way to reduce tool-related costs per cell. In order to optimize the throughput in a cell production line, both, front-end (chemical and thermal processes) and back-end (metallization and classification) processes should have equal capacity. Fig. 23 summarizes the expected throughput of cell production equipment, with synchronized front-end and back-end throughput processes anticipated by 2028.

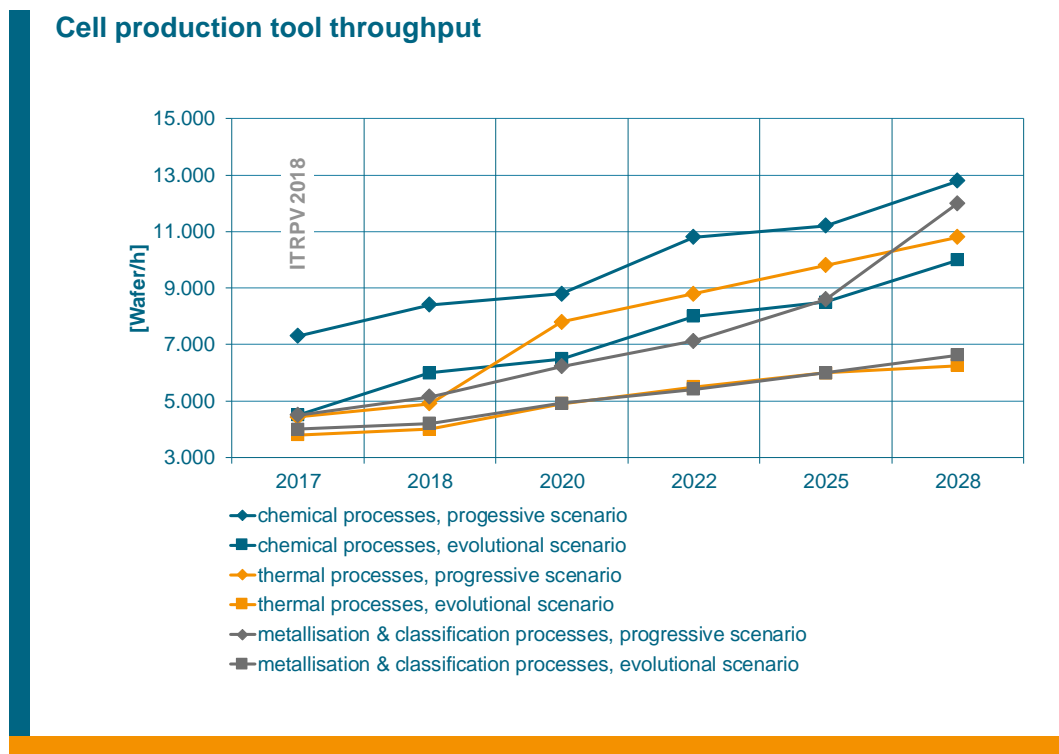


Fig. 23: Predicted trend for throughput per tool cell production tools.

Metallization tools with throughputs of > 5000 wafers/h are available on the market today. Further improvements in this field will depend strongly on the progress made with the screen printing technology that currently focuses on smaller line width and lower paste consumption. A maximum of > 10000 wafers/h is expected by 2028 for front- and back-end tool sets.

Wet chemical processing is still leading the throughput development with new machines enabling > 8000 wafers/h already in 2018. Two scenarios are considered for a discussion of this topic in more detail. The standard scenario reflects the evolutionary optimization approach, which is suitable for batch as well as in-line equipment (the evolutionary scenario). The progressive scenario also enables in-line or cluster line layouts but combines this with fairly new automation concepts and potentially higher process throughputs. Both scenarios are based on the achievement of substantial improvements through new tools, which are necessary to reduce depreciation and labor costs. More optimistic forecasts in previous editions have been offset by the current investment cycle. New “high throughput” equipment has been installed since 2016 on a large scale in mass production during the current investment cycle. Nevertheless, manufacturers are also working in existing lines on continuous process improvements by improving existing tool sets. In addition, the implementation PERC process upgrades is also accompanied by implementing new machines.

Single tools with increased throughput in chemical and thermal processing can be implemented, especially in cluster lines as replacements or upgrades as for PERC. New lines will be equipped from the beginning with the new tool concepts that matured during the last years in newly built production lines.

Increasing the tool throughput is also a measure for manufacturing cost reduction in module manufacturing. The expected throughput trend for key equipment in module front end and back end are summarized in Fig. 24.

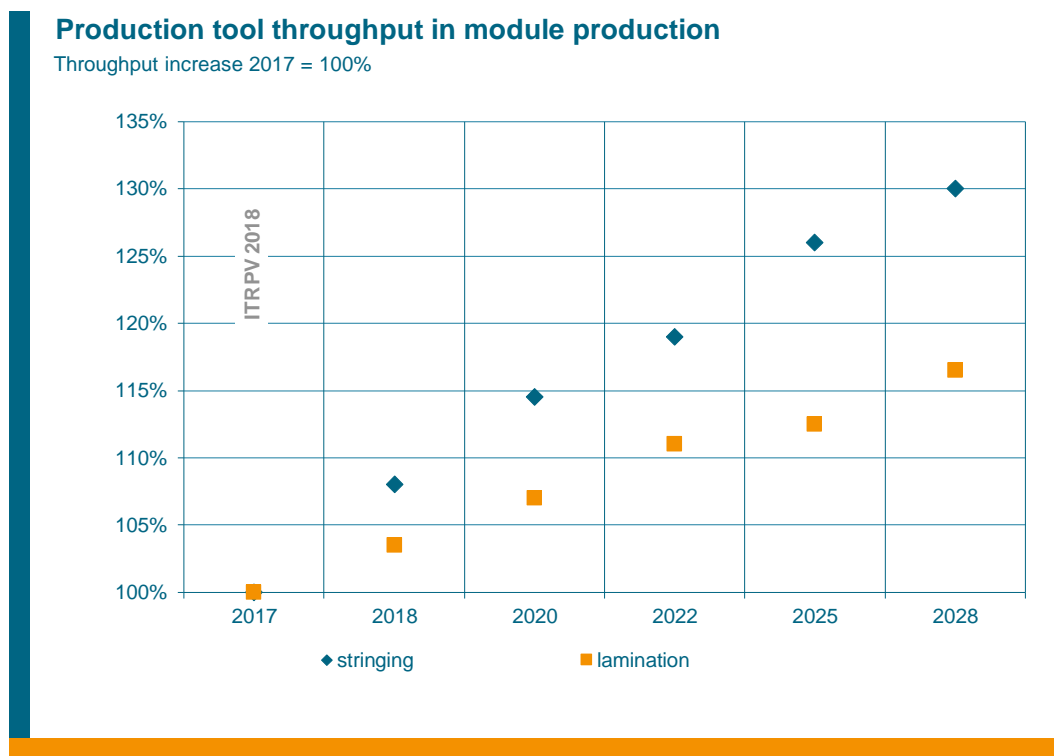


Fig. 24: Trend in tool throughput for cell stringing and module lamination.

In 2028 the throughput of stringing and lamination tools is expected to increase to 130% and about 115% respectively of the 2017 values.

In order to reduce the floor space and hence the cost of module manufacturing, the equipment should occupy less floor space and achieve higher throughput. This should be possible by combining continuous improvements and new developments, particularly for connection and encapsulation processes. For the latter process, new encapsulation materials with shorter processing times would be desirable.

## 5.2.2. Processes – technology

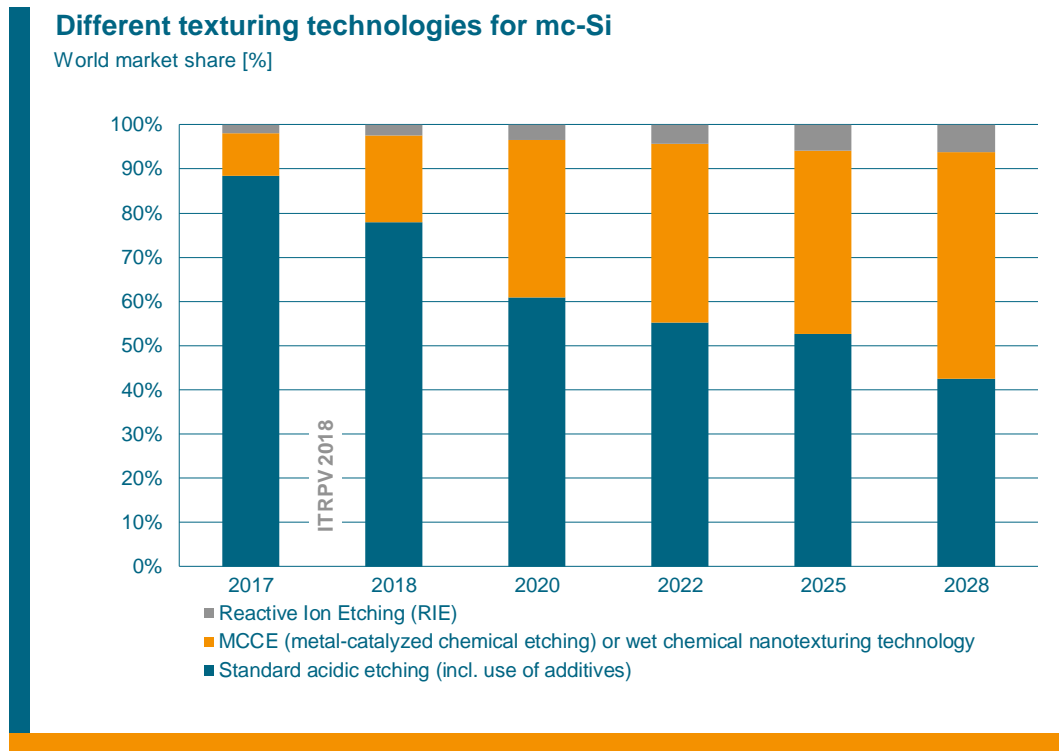


Fig. 25: Expected market share of different texturing methods for mc-Si.

The first production process in cell manufacturing is texturing. Reducing the reflectivity is mandatory to optimize cell efficiency. The expected market share of different texturing methods for mc-Si is shown in Fig. 25. Acidic texturing, a wet chemical process, is mainstream in current mc-Si cell production and is expected to stay mainstream. Wet chemical processing is a very efficient and cost optimized process especially due to its high throughput potential as discussed in Fig. 23. Standard acidic texturing including the use of additives is expected to stay the mainstream until 2025. Especially the application of additives enables good texturing of DWS mc-Si material. Metal catalyzed chemical etching (MCCE) or wet chemical nano-texturing technologies are expected to gain market share of up to 50%. The performance of the different wet chemical etch-processes in texturing the DWS mc-Si wafers will decide which set up will make the race. Reactive ion etching (RIE) is not expected to exceed 6% market share in 2028 due to the higher cost.

Solar cell recombination losses on the front and rear sides of the cell, as well as recombination losses in the crystalline silicon bulk material, must be reduced in line with high-efficiency cell concepts. The recombination currents  $J_{0\text{bulk}}$ ,  $J_{0\text{front}}$ ,  $J_{0\text{rear}}$ , indicating the recombination losses in the volume, on the cell's front and rear side respectively, are a reasonable way to describe recombination losses. Fig 26 shows that all recombination currents need to be reduced. The values are in line with the assumptions of former ITRPV editions.

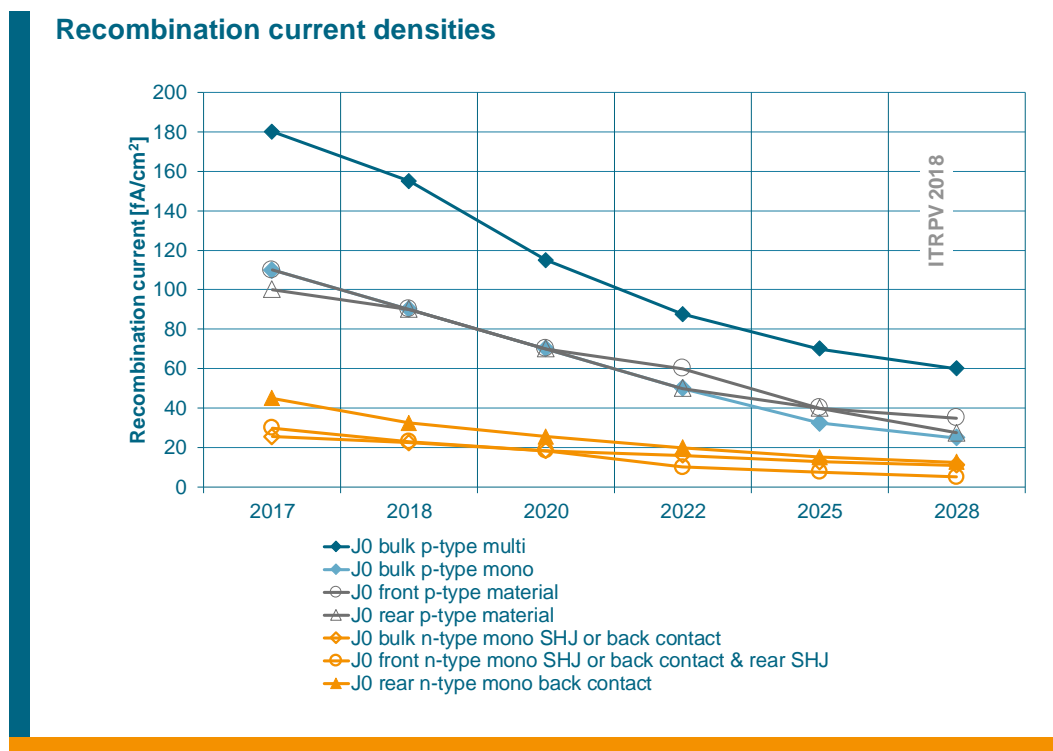


Fig. 26: Predicted trend for recombination currents  $J_0$ bulk,  $J_0$ front,  $J_0$ rear for p-type and n-type cell concepts.

Recombination currents can be measured as described in the literature [13], or they can be extracted from the IV curve if the other  $J_0$  components are known.

The improvement of the silicon material quality for both, mono and multi will continue. This should result in a reduction of the  $J_0$ bulk value to 60 fA/cm<sup>2</sup> for multi and around 30 fA/cm<sup>2</sup> for mono. N-type mono wafers display a  $J_0$ bulk value of <30 fA/cm<sup>2</sup>, which is expected to be further reduced to about 10 fA/cm<sup>2</sup> within the next 10 years.

Reductions of  $J_0$ bulk will result from improvements to the crystallization process (see 5.3). The introduction of improved casted silicon materials (e.g. HPmc-Si, mono-like-Si) resulted in lower bulk recombination currents for this material type.

$J_0$  values of front and rear surfaces are similar for different bulk materials. This  $J_0$  values are expected to be reduced by up to 70% of the current values by 2028.

Rear-side recombination current values below 200 fA/cm<sup>2</sup> cannot be attained with an Al Back Surface Field (BSF). Therefore,  $J_0$ back improvement is linked directly to cell concepts with passivated rear side.

Since 2012, several cell concepts using rear-side passivation with dielectric layer stacks have been introduced to production processes (PERC / PERT technology). Fig. 27 shows the predicted market shares of different rear-side passivation technologies suitable for n-type and p-type cell concepts.

PECVD Al<sub>2</sub>O<sub>3</sub> in combination with a capping layer is and will be the most widely used technology for PERC cell concepts. Another technology, ALD Al<sub>2</sub>O<sub>3</sub> deposition in combination with capping layers, is not expected to reach large market-penetration. PECVD SiON<sub>x</sub>/SiNy will disappear.

### Different rear side passivation technologies

World market share [%]

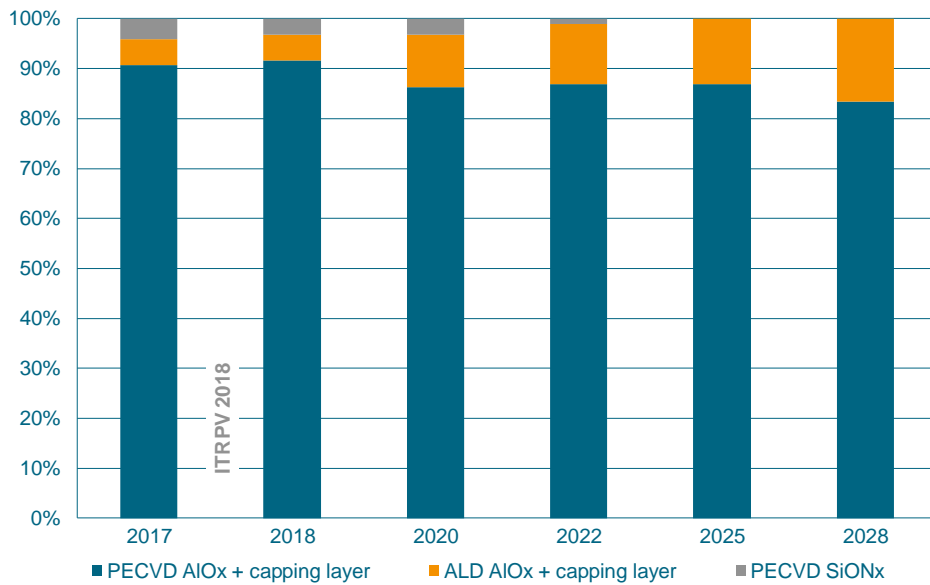


Fig. 27: Predicted market shares for AIOx-based rear-side passivation technologies.

### Emitter sheet resistance for phosphorous doping for p-type cells

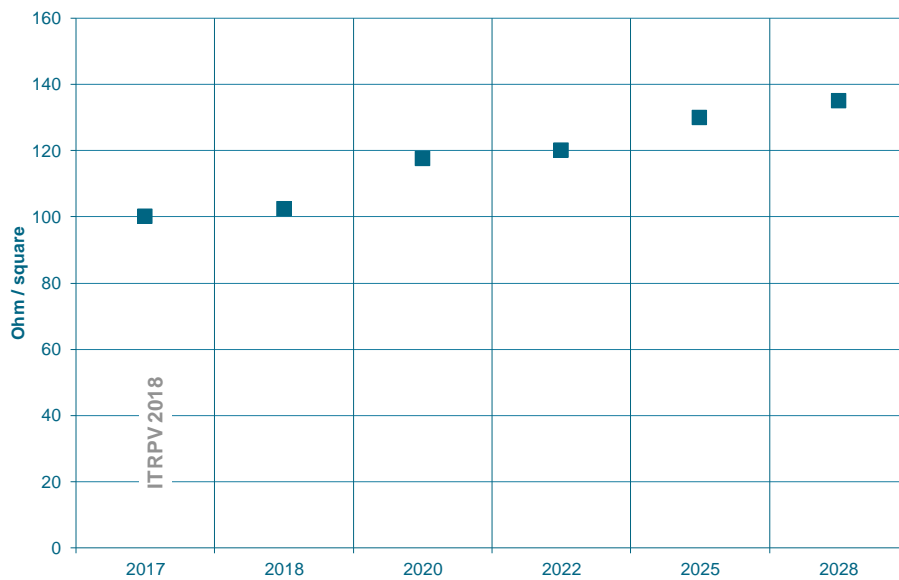


Fig. 28: Expected trend for emitter sheet resistance.

One parameter that influences recombination losses on the front surface is emitter sheet resistance. The predicted trend for n-type emitters is shown in Fig. 28. It can be seen that an emitter sheet resistance of about 100 Ohm/square is mainstream in today's industry.

Increased sheet resistances above 100 Ohm/square can be realized with and without selective emitters. If a selective emitter is used, sheet resistance shall refer only to the lower doped region, whereas J0front includes all relevant front-side parameters (emitter, surface, contacts).

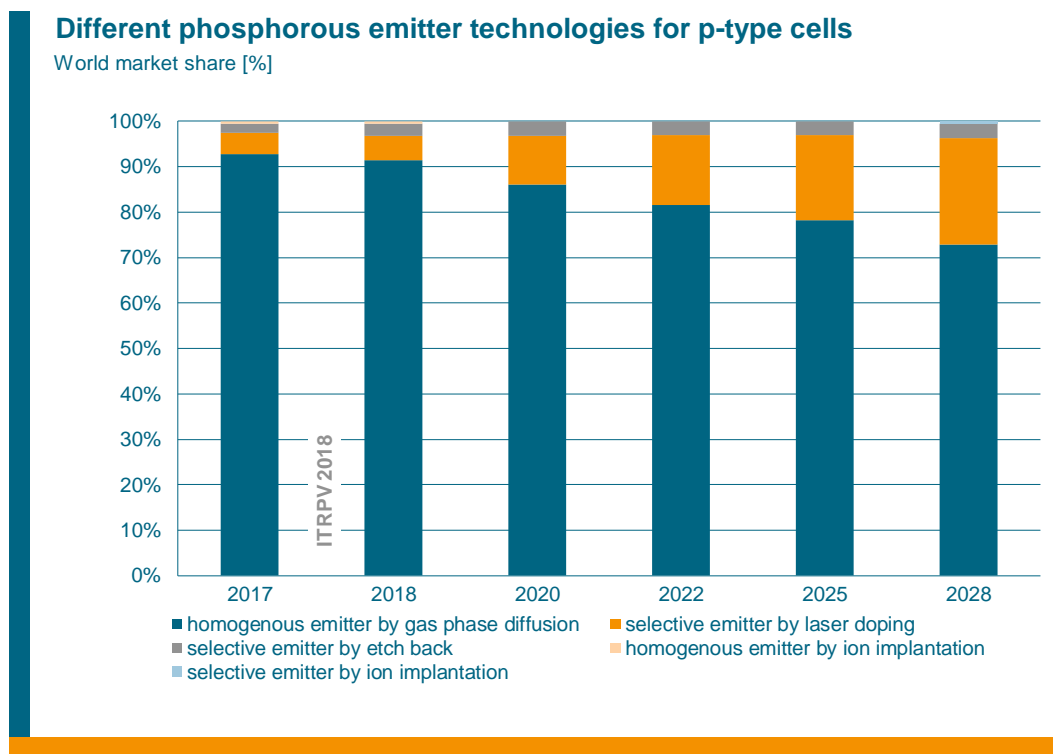


Fig. 29: Expected world market share for different Phosphorous emitter technologies for p-type cells.

Fig. 29 shows the expected world market share of different technologies for Phosphorous doping in p-type cell processing. Homogeneous gas phase diffusion is a mature, cost efficient doping technology and will remain the mainstream for the years to come, despite the availability of other technologies.

Nevertheless, selective emitter processes are expected to be used in mass production with shares of >10% by 2020. Ion implantation for homogeneous doping will stay niche application with <1% share. Like in the 7<sup>th</sup> and 8<sup>th</sup> edition of the ITRPV, we discuss below technologies for boron doping, especially for n-type cells. Fig 30 shows the expected market share for the different boron doping technologies.

In line with the findings of the last editions we expect that the currently most widely used BBr thermal diffusion technique will stay mainstream. Ion implantation is supposed to be applied in production but at with low market share of <5%. Alternative doping technologies such as APCVD/PECVD of doped layers in combination with thermal diffusion are expected to have a high potential for implementation until 2027.

Front metallization is a key process in the production of c-Si solar cells. New front-side metallization pastes enable the contacting of the previously discussed low-doped emitters without any significant reduction in printing process quality.

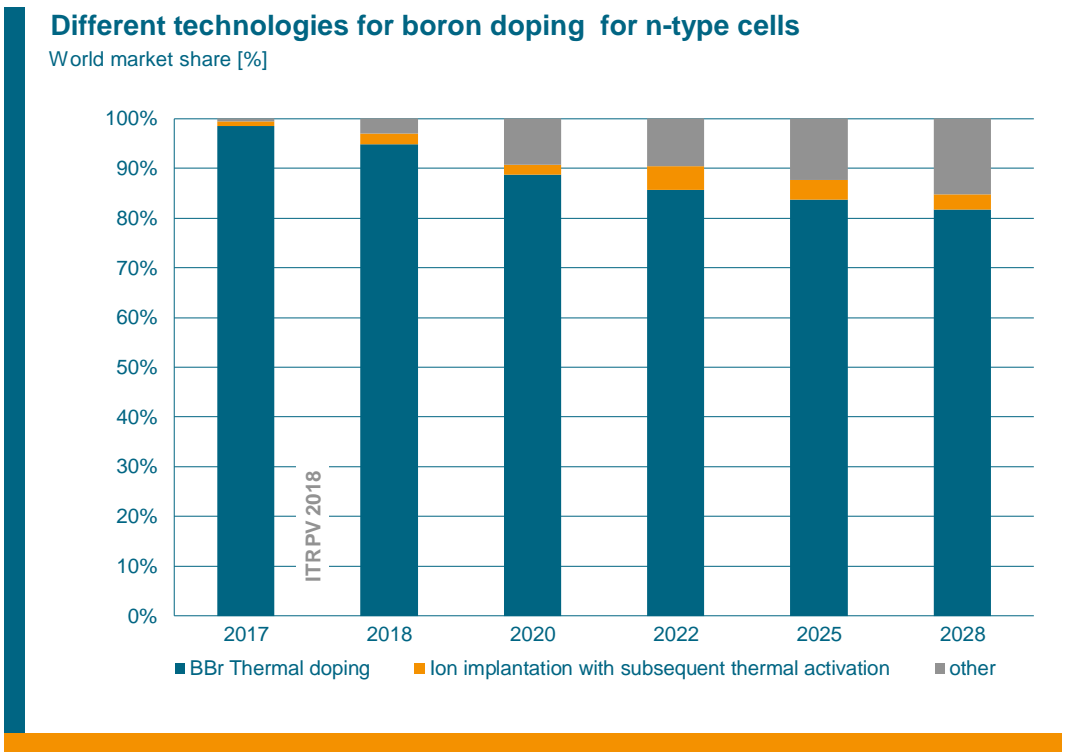


Fig. 30: World market share for different technologies for boron doping (n-type cells).

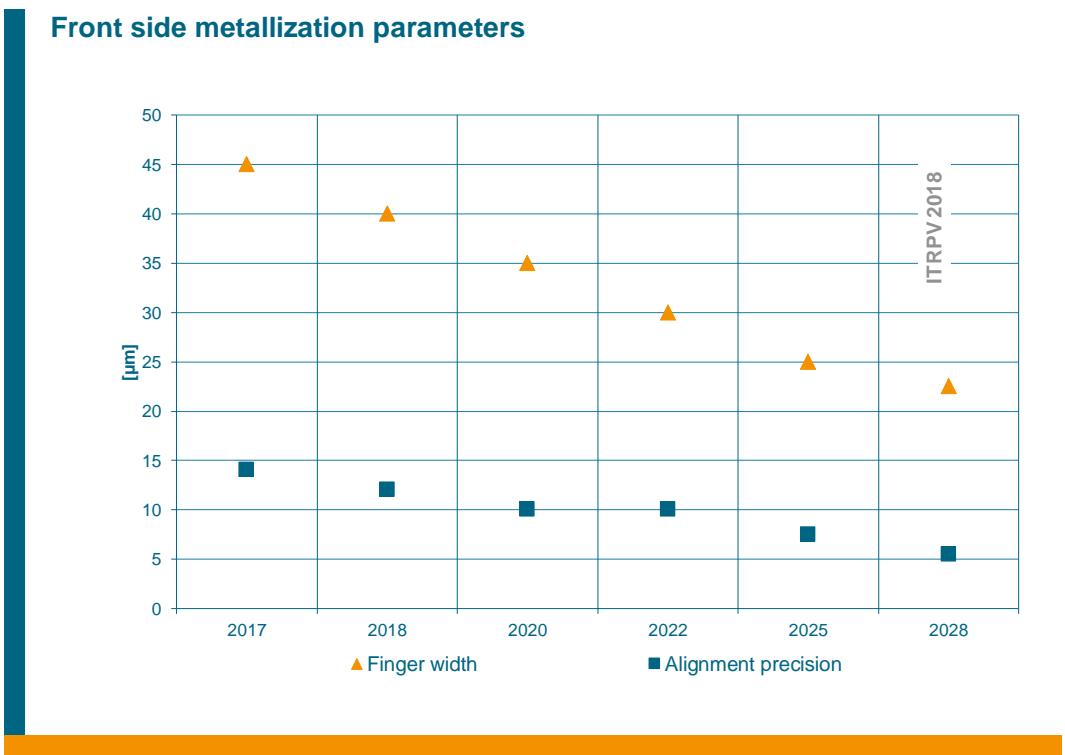


Fig. 31: Predicted trend for finger width and alignment precision in screen printing. Finger width needs to be reduced without any significant reduction in conductivity.



A reduction in finger width is one method yielding in efficiency gain and cost reduction, but only if it is realized without significantly increasing finger resistance. Furthermore, contact with a shallow emitter needs to be established reliably. One possible way to achieve these goals is to use a selective emitter structure, preferably without increasing processing costs.

Finger widths of 40  $\mu\text{m}$  will be standard in 2018. A further reduction to 23  $\mu\text{m}$  appears possible over the next 10 years. Reducing finger width reduces shadowing, but a trade-off has to be made to maintain conductivity if the roadmap for silver reduction as discussed in 5.1.2 will be executed.

Different approaches for high quality front side print exist. Fig. 32 summarizes the available technologies and their estimated market share during the next 10 years.

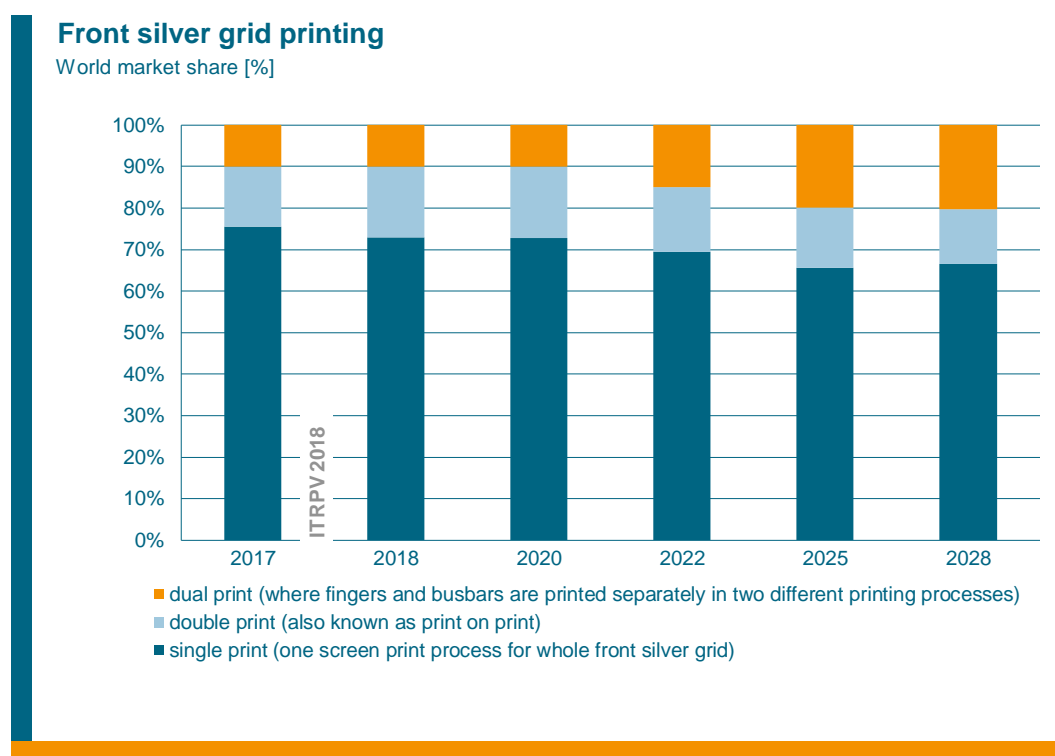


Fig. 32: Expected market share of different front side printing techniques.

Single print technology is mainstream, followed by double printing. Double printing requires an additional printing step and exact alignment. A third, more robust technology — the dual print — separates the finger print from the busbar print, enabling the use of busbar pastes with less silver. New busbar less cell interconnect techniques can even omit the busbars completely. Therefore, for reliable module interconnection, and for future applications as bifacial cells, a good alignment accuracy is important in metallization — an alignment accuracy of about 10  $\mu\text{m}$  (@ $\pm$  3 sigma) will be required from 2020 onwards as shown in Fig 31.

The expected share of different technologies for front side and rear side metallization are shown in Fig. 33a and 33b respectively. Fig. 33a shows that classical screen printing is expected to remain the mainstream technology for the years to come in front side metallization. Stencil printing, which can be used with existing screen printing equipment, started on small scale in mass production. Plating technologies are expected to be introduced in mass production in 2020, a market share of about 10% is expected for 2028 — again a delay regarding former ITRPV editions.

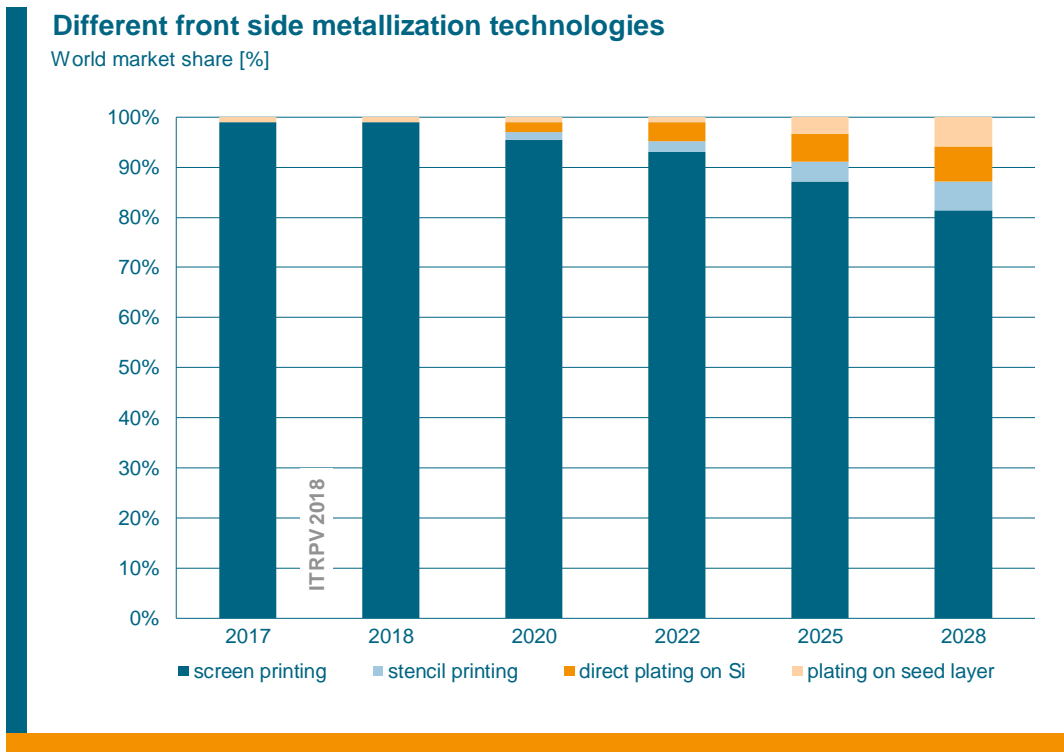


Fig. 33a: Predicted trend for different front side metallization technologies.

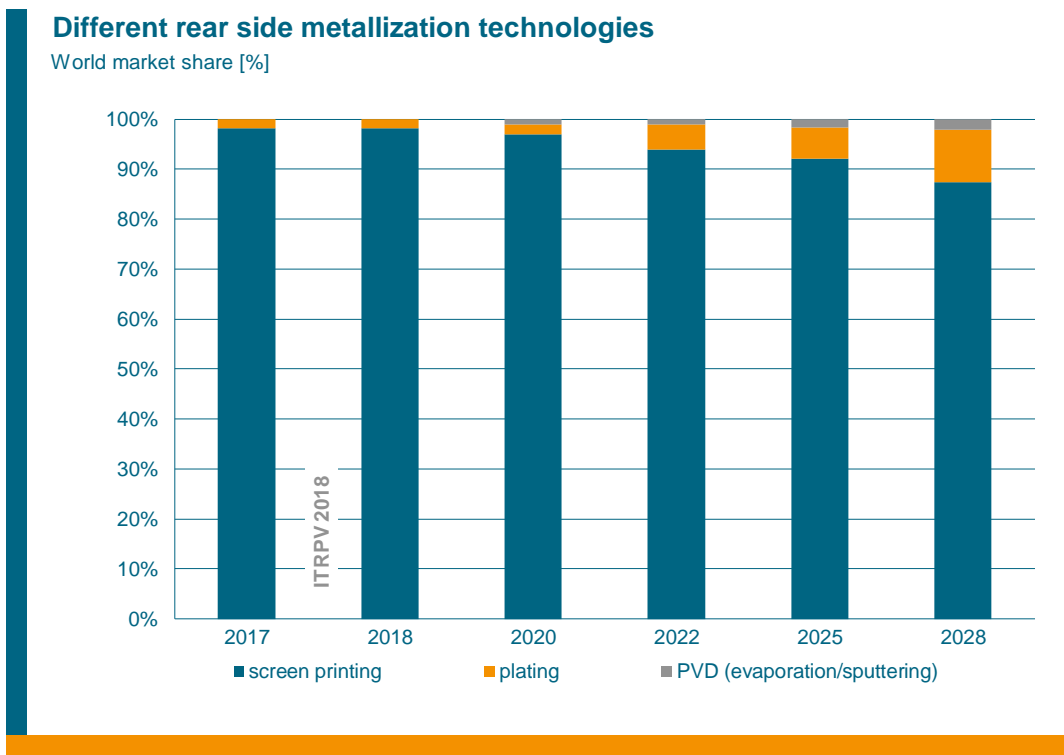


Fig. 33b: Predicted trend for different rear side metallization technologies.

Screen printing as well is expected to stay mainstream in rear side metallization for the next years as shown in Fig. 33b. Plating, especially used for rear side contact cells, is expected to gain slowly market

share of around 10% in 2028. Physical vapor deposition (PVD) by evaporation or sputtering is still expected to appear as niche application.

As mentioned above, reducing the finger width requires a tradeoff – a current trend in metallization relates to the number of busbars (BB) used in the cell layout. Fig. 34 shows the expected trend. We see that the 3-BB layout, is being phased out and will be fast replaced over the next years by layouts with 4, 5, 6 and more BBs - and by BB-less layouts. BB-less technologies support minimum finger widths as shown in Fig. 31. Nevertheless, this will require new interconnection technologies in module manufacturing that cannot be implemented by simple upgrading of existing stringing tools.

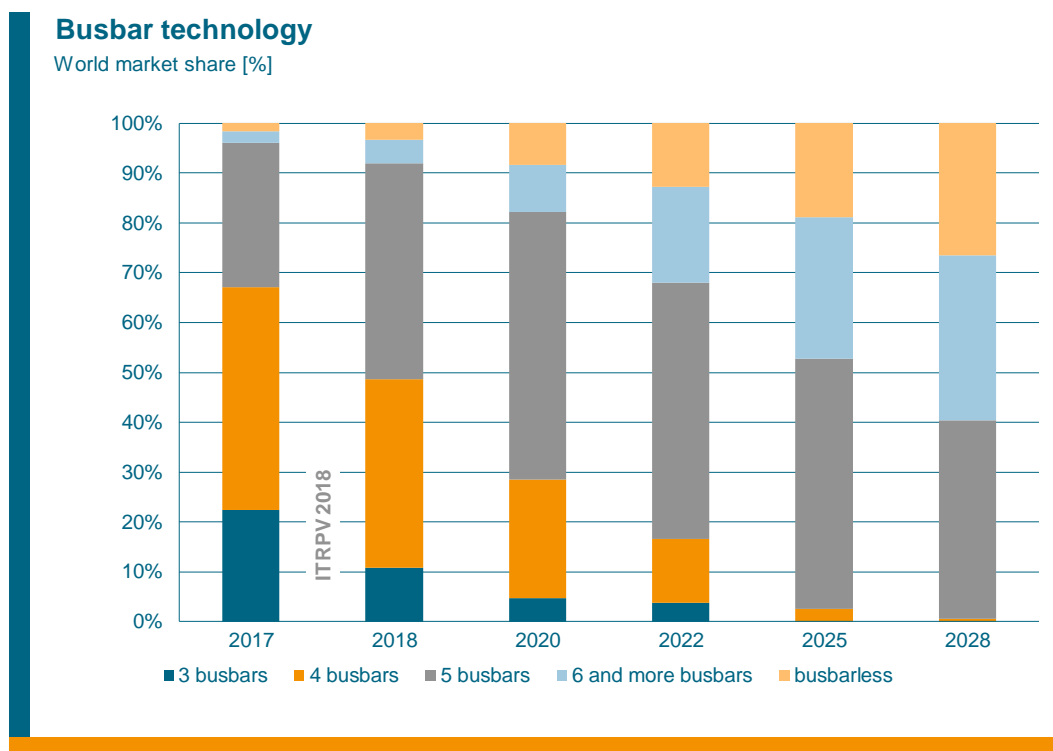


Fig. 34: Worldwide market share for different busbar technologies.

It is crucial to get as much power out of the assembled solar cells as possible. The cell-to-module power ratio is a good parameter to describe this behavior. It is defined as module power divided by cell power multiplied by the number of cells (module power / (cell power x number of cells)). This ratio was 2017 at 99.5% for mc-Si cell technology (acidic texturing) and at 98% for mono-Si cell technology (alkaline texturing), as shown in Fig. 35.

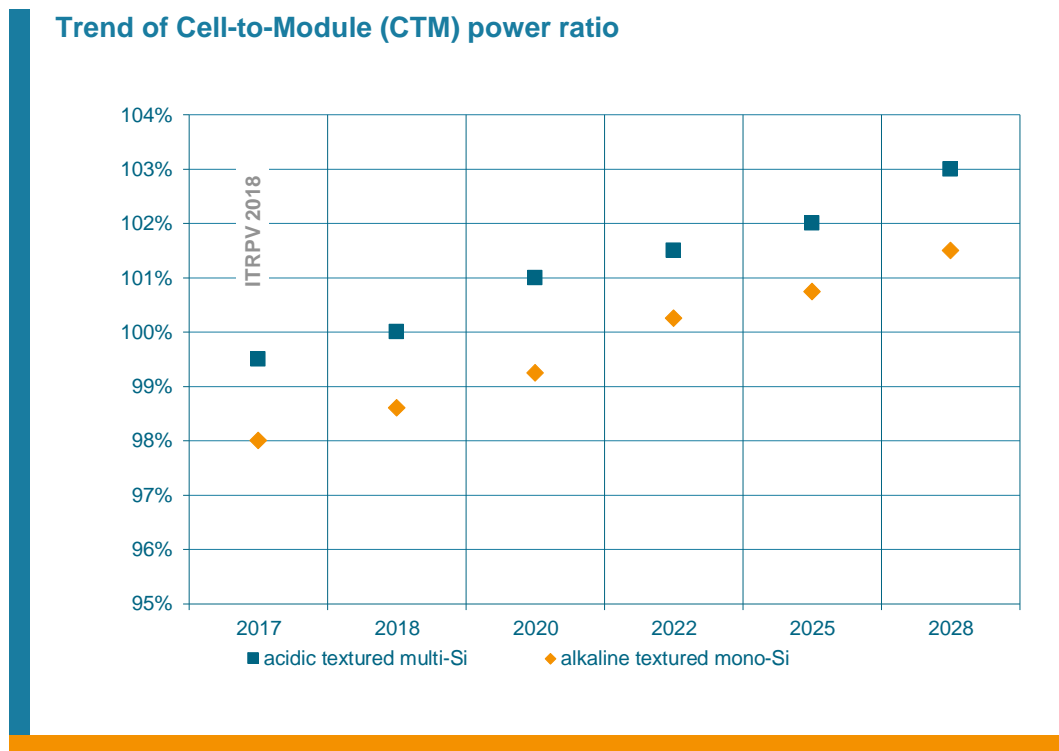


Fig. 35: Expected trend for the cell-to-module power ratio.

The cell-to-module power ratio is expected to exceed 100% for both cell types but slightly delayed relative to the 8<sup>th</sup> edition. This implies that the power of the finished module will exceed the power of the cells used in the module. Such effects will be enabled by smart interconnection techniques and further improvements of light management within the module as a means of redirecting light from inactive module areas onto active cell areas. The introduction of new interconnection and encapsulation technologies (e.g. narrower ribbons, encapsulation materials with improved UV performance, etc.) will result in further improvements that will enable additional power gains.

The junction box is the electrical interface between the module and the system. We found that the internal electrical connection of the bypass diodes is and will be done mainly by soldering, welding is gaining market share over the next years whereas clamping, the third technology, will be used less in the future. Also, we found that the current single junction box concept is expected to shift to multiple junction box as mainstream from 2020 onwards.

In-line process control in cell and module production lines becomes more and more important to ensure high production yields, high average efficiencies, perfect optical appearance and longtime product reliability. Fig.36a and Fig. 36b summarize the assumptions about in-line cell process control of selected key process parameters. Automatic inspection (AI) of Incoming wafer is assumed to be in use in about 25% of all cell production lines. Sorting out off-spec material is important to ensure high cell production yields, Measurement systems for sheet resistance will be implemented more and more in contemporary production lines for diffusion process monitoring - 50% of the production lines will be using the in 2025. The control of the front side antireflective (AR) layer is in use at about 30% of production lines. Nevertheless, the penetration in 2025 is expected to reach 50%. In-line printing control is becoming more important in modern production lines.

The trends for AI at cell test are summarized in Fig. 36b.

### In-line process control

World market share [%]

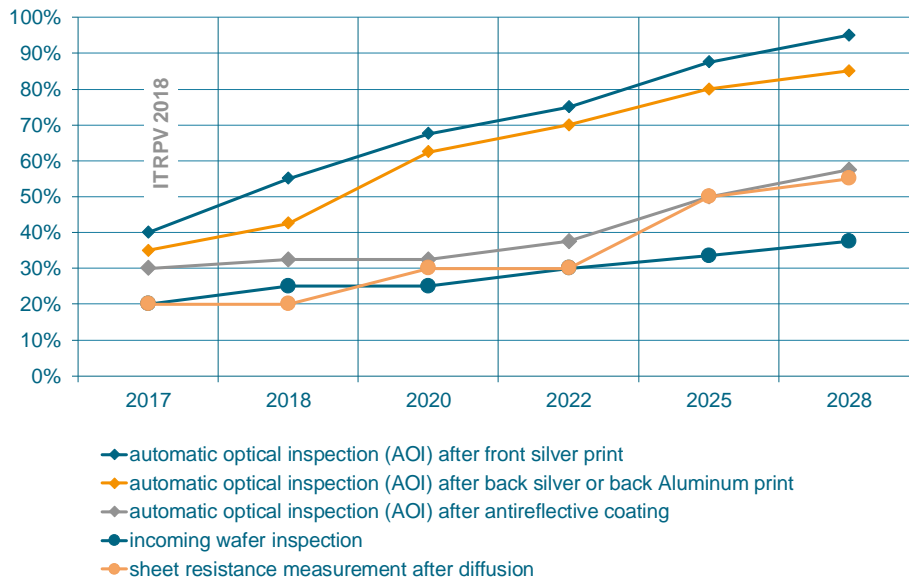


Fig. 36a: Market share of in-line process control for incoming wafer quality, sheet resistance, antireflective coating, and for printing quality at rear and front side printing.

It is expected that in future >80% of lines will be equipped with such systems. The trend is different from last year's survey results.

### Process control in cell tester / sorter

World market share [%]

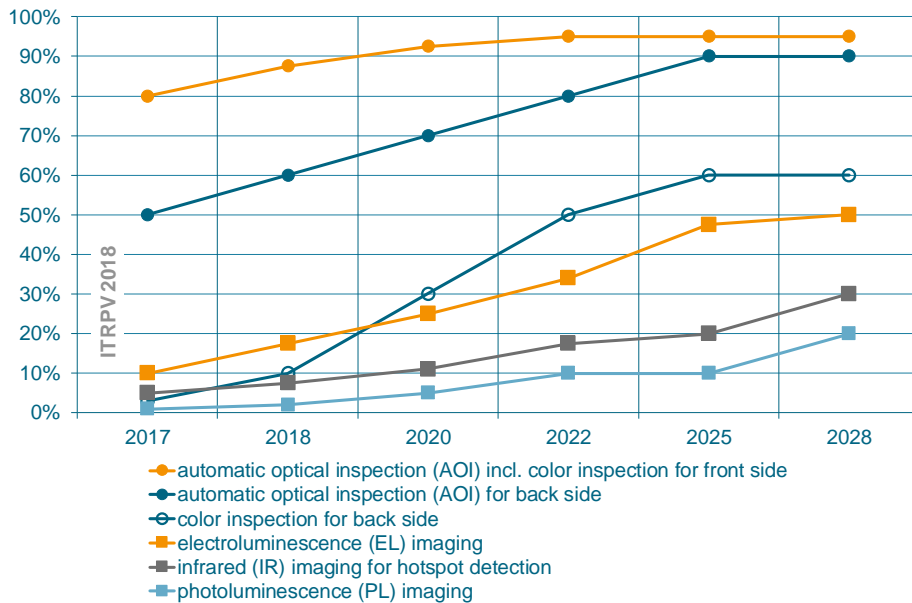


Fig. 36b: Market share of different in-line Automated Inspection (AI) systems for process control at cell test.

AOI incl. color inspection of the front side at cell test is standard in today's cell production lines. On top of optical inspection, we see an increasing share of IR, EL, and PL systems. The latter considered to have the lowest implementation share with <5% today and only 20% in 2028.

The trends for in-line testing and manufacturing execution systems (MES) in module production lines are summarized in Fig. 37. EL inspection of modules is standard even today with >95% in 2028. A similar trend is visible in AOI of cells in the stringers. IR and cell color inspection in module production are expected stay on low level as those inspection is already done at cell test.

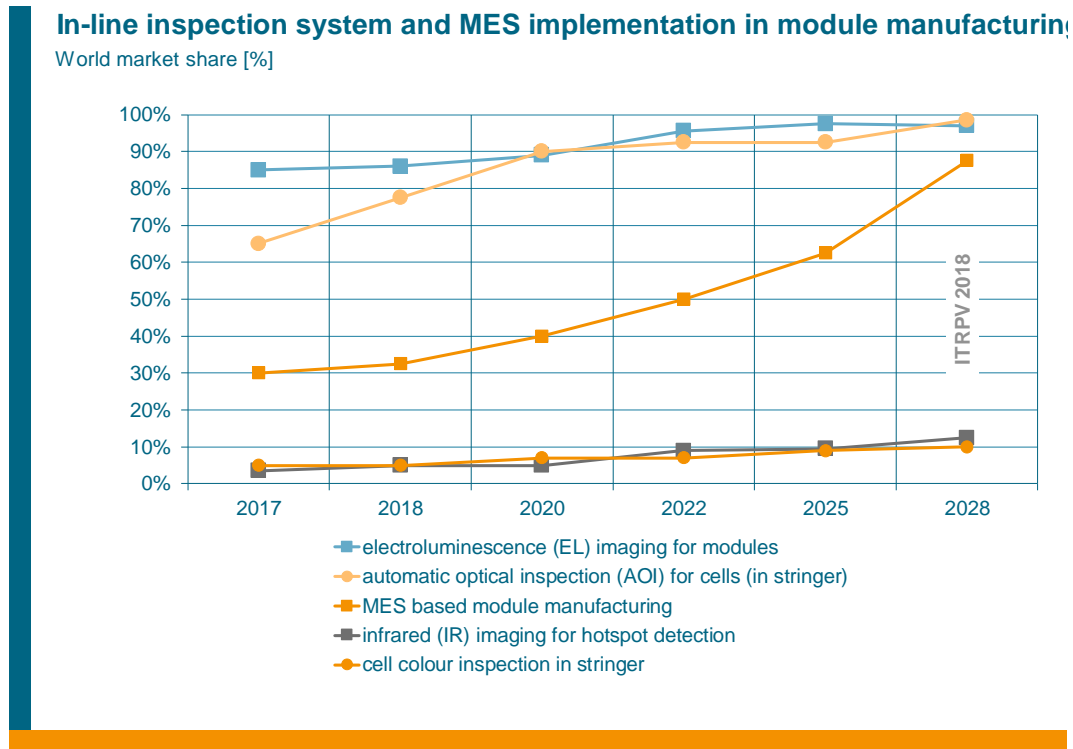


Fig. 37: Trends of in-line inspection systems and MES implementation in module production lines.

The implementation of MES progresses – today's share of 30% is predicted to increase systematically to above 80% in 2028. This is a clear sign towards further automation in module manufacturing.

### 5.3. Products

Casted materials are assumed to have 52% of today's wafer market of c-Si silicon solar cell manufacturing and it had an assumed market share in 2017 of about 60% vs. 40% for mono. This is slightly different to the assumptions of Solar Media [14]. However, it is assumed that the market share of casted wafer types will further shrink to below 40% in 2028. Simply distinguishing between mono-Si and mc-Si, as was done some years ago, this is insufficient. The c-Si materials market is further diversifying, as shown in Fig. 38. High-performance (HP) mc-Si material dominates the casted silicon market. Due to its excellent performance, this material is about to replace conventional mc-Si completely. Mono-like-Si will stay present but at a negligible share.

Mono-Si will make further gains over casted materials and will attain an assumed share of 61% in 2028. This trend of increased mono-Si market share is in line with the assumptions of the past ITRPV editions. We predict a market share of p-type mono-Si of about 30% for the years to come and increase of n-type mono-Si to about 28% - similar as assumed in the 8<sup>th</sup> edition. This is mainly due to the

tremendous progress in stabilizing p-type mono degradation performance.

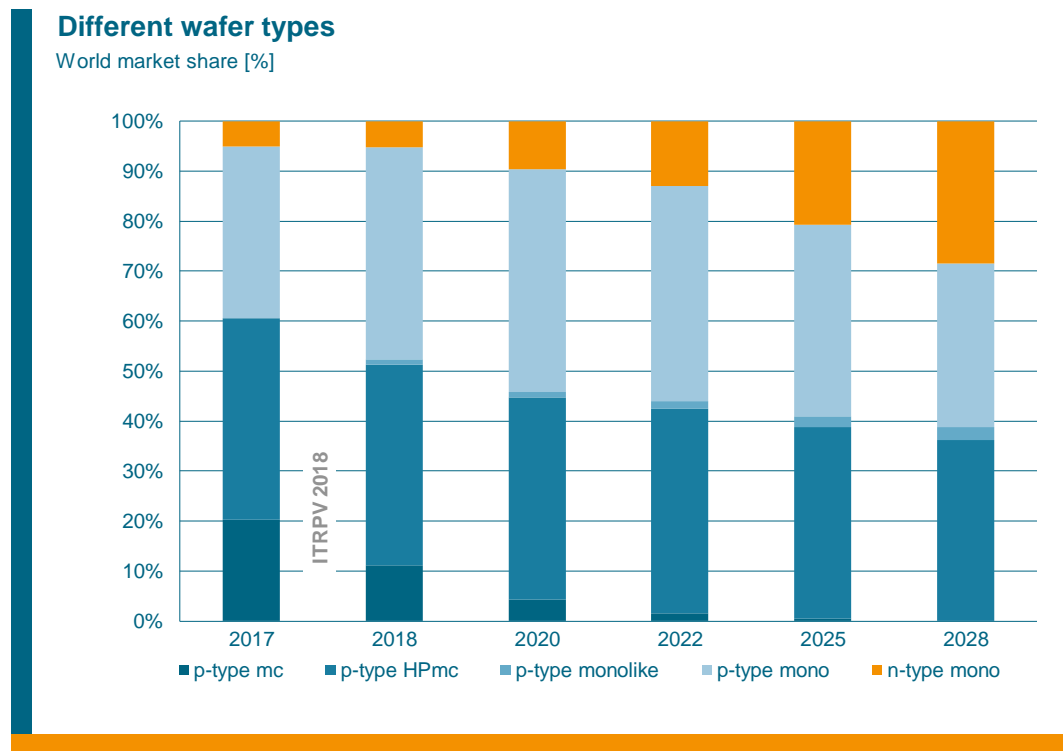


Fig. 38: World market shares for different wafer types.

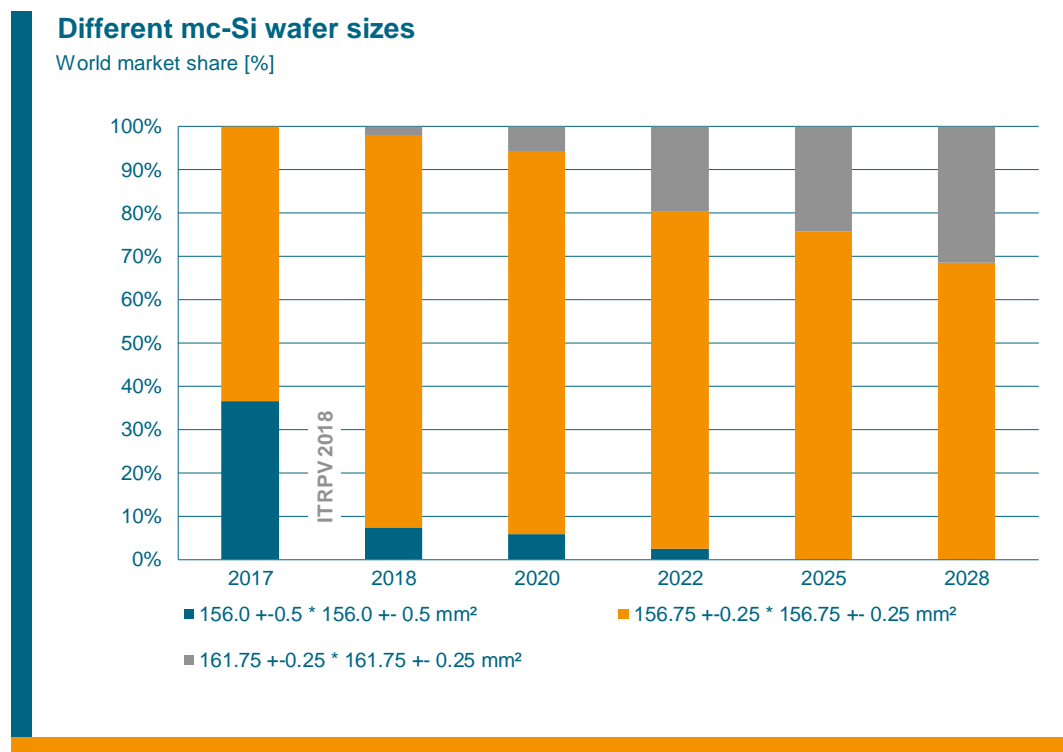


Fig. 39: Expected trend of mc-Si wafer size in mass production.

Fig. 39 and Fig. 40 show the ITRPV survey results about the market share of different wafer dimensions for mc-Si and mono-Si wafers respectively.

The new wafer formats first appeared in 2015. The move from 156x156mm<sup>2</sup> to the slightly larger format of 156.75 x 156.75 mm<sup>2</sup> in mass production started 2016. The transition to 156.75 x 156.75 mm<sup>2</sup> was faster for mono-Si: 2017 share of the larger format is shown with 90% for mono-Si vs. 63% for mc-Si. The format is clear mainstream in the industry for both material types. An even larger format was introduced by one cell and module manufacturer in 2016. We assume similar, larger format of 161.75 x 161.75 mm<sup>2</sup> will also be introduced in the market for mc-Si and mono-Si. Standardization of wafer dimensions is highly recommended in order to enable tool manufacturers to provide the right tools and automation equipment. The dimension change for mono-Si is assumed to go in parallel with an increase in diameter of the pseudo square wafers: 210 mm are mainstream today with >90% market share.

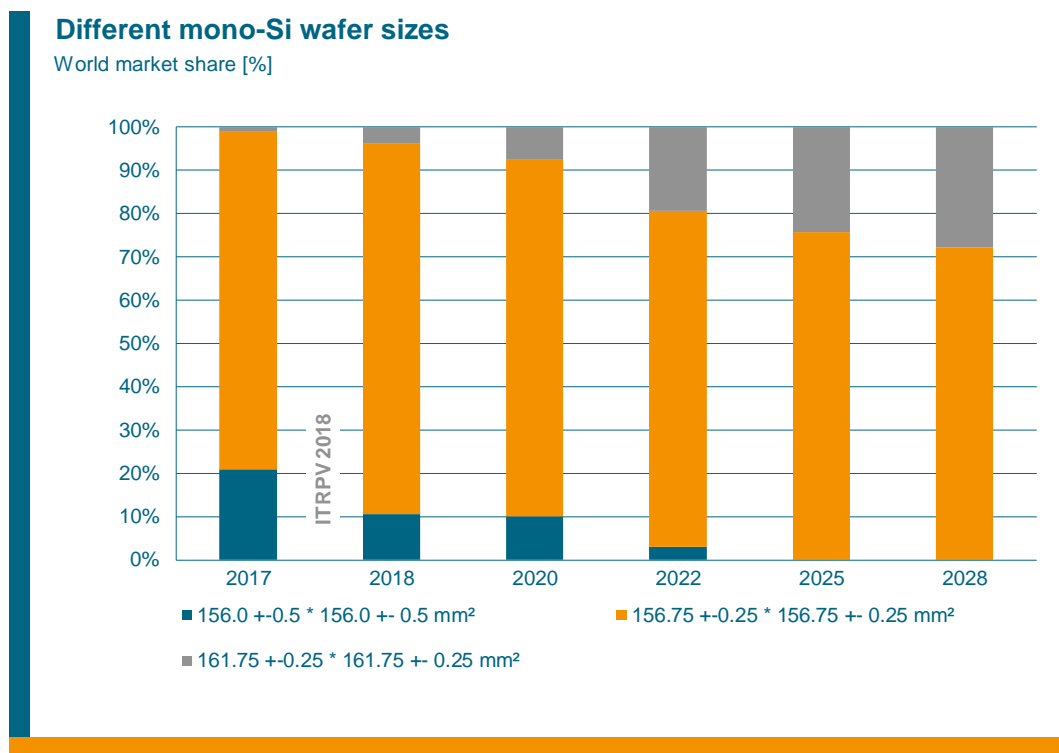


Fig. 40: Expected trend of mono-Si wafer size in mass production.

The roadmap also confirms that pseudo square wafers will dominate the market over full square wafers. Nevertheless, we expect that the share of full square wafers will increase to about 5% in 2020 and to about 20% in 2028.

The current edition of the ITRPV confirms a mainstream market for double-sided contact cell concepts; within this market, PERC/PERT/PERL cells will gain significant market share over BSF cells and will be mainstream after 2020, as can be seen in Fig. 41. Secondly, heterojunction (HIT/HJT) cells are expected to gain a market share of 10% in 2025 and 15% by 2028. The share for rear-side contacted cells is not expected to gain significant market share: from 2017 2% to about 10% in 2028. Si-based tandem cells are expected to appear in mass production operations in 2020.



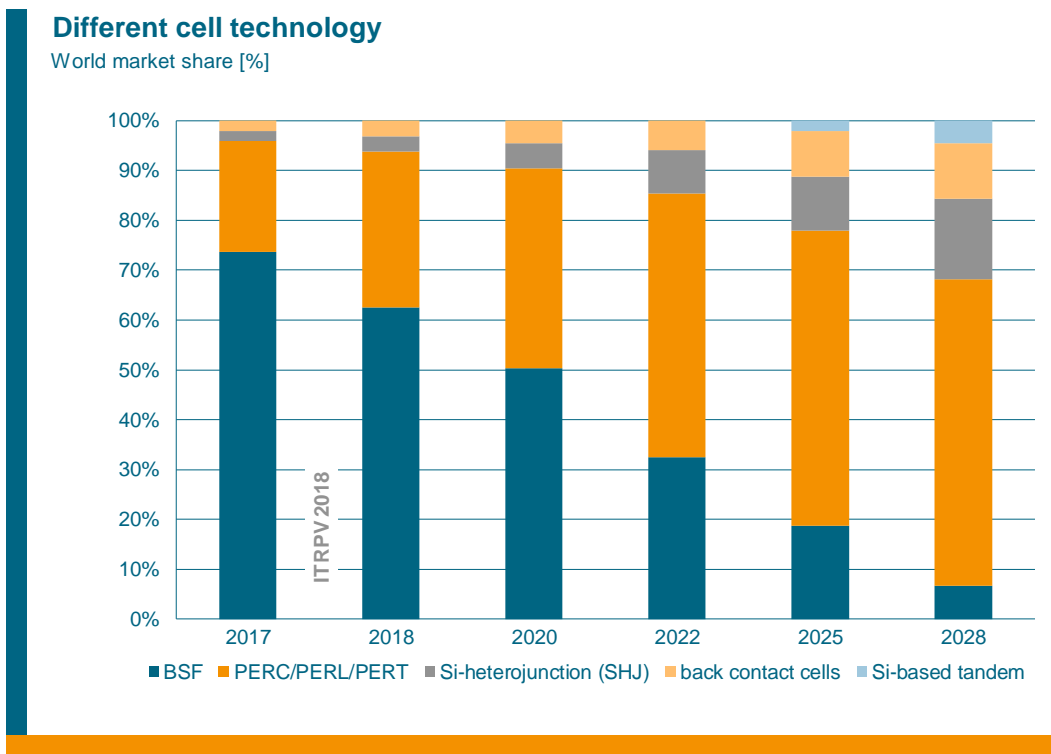


Fig. 41: Worldwide market shares for different cell technologies.

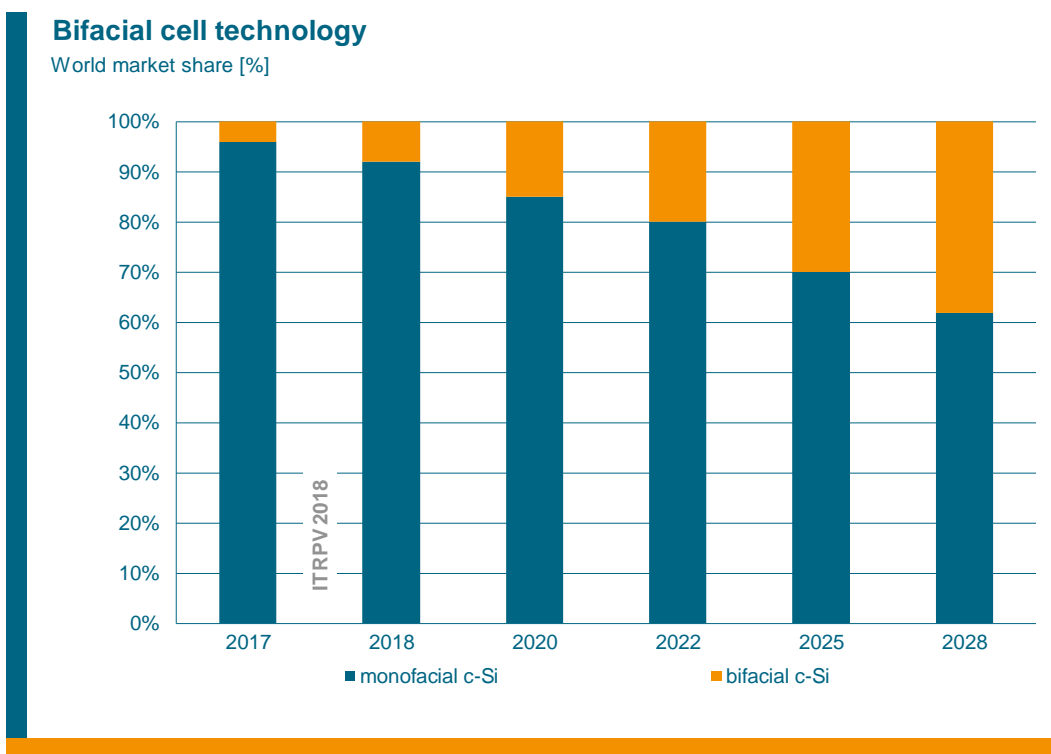


Fig. 42: Worldwide market shares for bifacial cell technology.

Furthermore, we expect that an increasing number of cells will be light-sensitive on both sides, so called bifacial cells. Our survey predicts that the percentage of bifacial cells will steadily increase to nearly 40% by 2028 as shown in Fig. 42.

Today most of modules are mono facial modules. As shown in Fig. 42 bifacial cells will gain market share. Fig. 43 shows the expected share of true bifacial modules. It is expected that bifacial cells will also be used in traditional mono facial modules. Nevertheless, we expect that the market share for bifacial modules will increase to more than 35% in 2028.

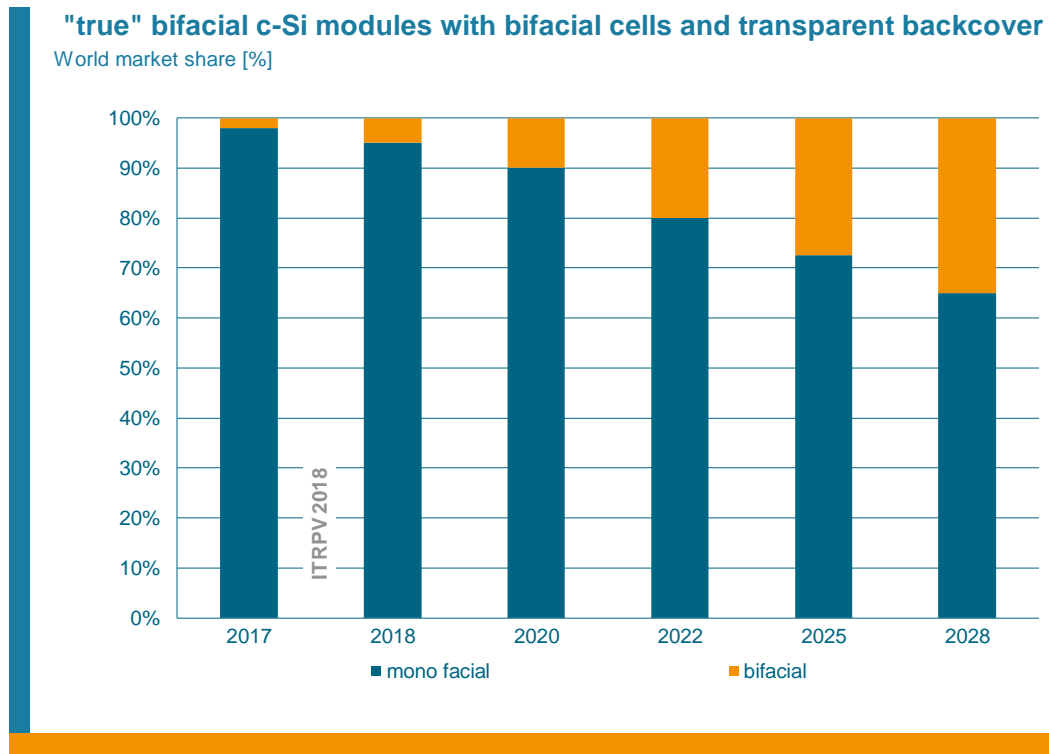


Fig. 43: Worldwide market shares for monofacial and "true" bifacial modules.

Fig. 44 shows the expected average stabilized cell efficiencies on state-of-the-art mass production lines for double-sided contact and rear-contact cells on different wafer materials. The plot shows that there is big potential for all technologies to improve their performance. N-type cells show the highest efficiency potential. Nevertheless, there will be nearly no efficiency delta for double-side contacted mono n- and p-type cells in the future. We found that p- and n-type mono cells will reach 23.5% with PERC/PERT/PERL processes. Other n-type-based cell concepts like HJT and back-contact cells, will reach higher efficiencies.

### Average stabilized efficiency values for Si solar cells (156x156mm<sup>2</sup>)

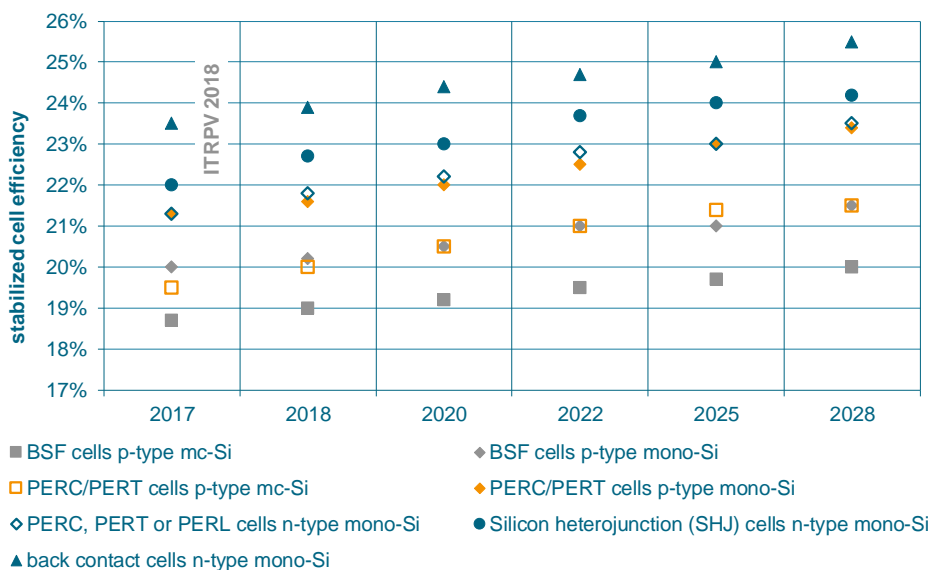


Fig. 44: Average stabilized efficiency values of c-Si solar cells in mass production (156 x 156 mm<sup>2</sup>).

Fig. 45a and Fig. 45b show the corresponding development of module power for typical 60- and 72-cell modules with 156 x 156 mm<sup>2</sup> cells, considering the cell efficiencies shown in Fig. 43 and the cell-to-module power ratio trend shown in the previous Section (Fig. 35). We assume acidic texturing for mc-Si and HP mc-Si and alkaline texturing for mono-Si. In addition, we consider pseudo-square wafers with diagonals of 210 mm as mono-Si material. Changes in module size are not considered.

It should be noted that for modules with high efficiency back-contact cells, which are not yet available on 156 x 156 mm<sup>2</sup> wafers, the module power values given in Fig. 45a represent equivalent values in order to enable a better comparison with double-side contact technologies. 60 cell Modules with PERC/PERT HP mc-Si will achieve module power classes of 325 W by 2028. Modules with mono-Si p-type PERC/PERT will reach 310 W in 2018 and will achieve a power output in the range of nearly 345 W by 2028, as shown in Fig. 44a. Modules with HJ cells are expected to reach in 2018 325 W and in 2028 355 W.

The calculated corresponding module powers for 72 cell modules are visualized in Fig. 45b. mc-Si p-type PERC modules will surpass 370 W power class and 415 W in 2028.

### Module Power for 60-cell (156x156mm<sup>2</sup>) module

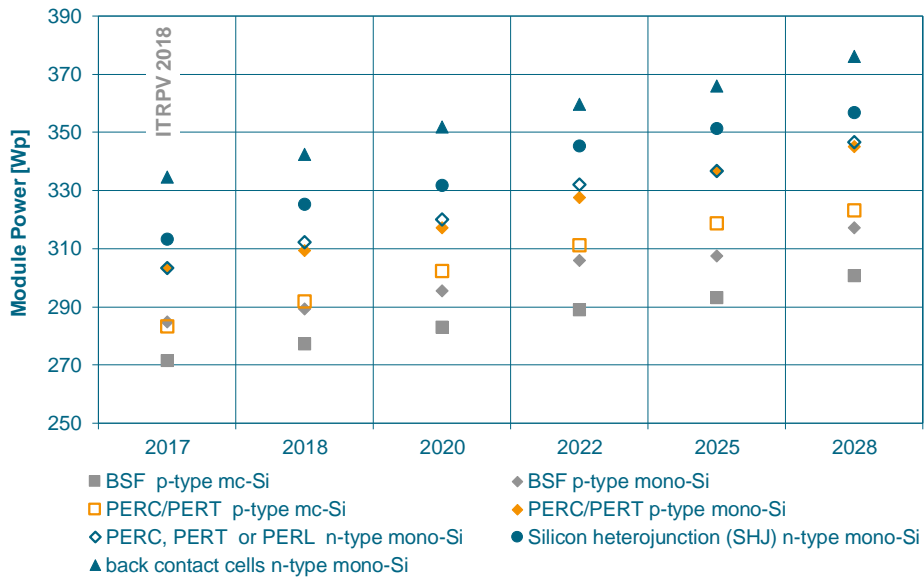


Fig. 45a: Predicted trend curve for module power of 60-cell modules for different c-Si cell types.

### Module Power for 72-cell (156x156mm<sup>2</sup>) module

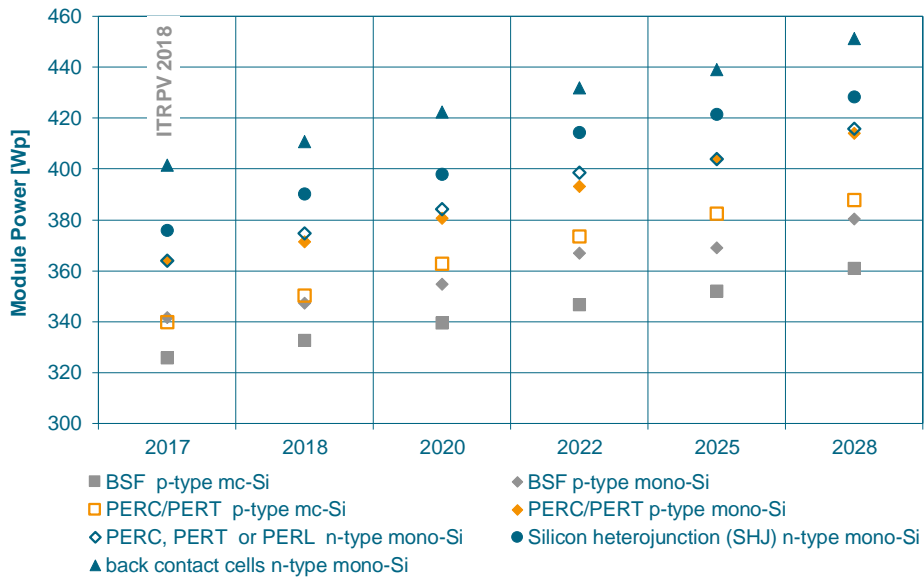


Fig. 45b: Predicted trend curve for module power of 72-cell modules for different c-Si cell types.

Modules that use half-sized cells rather than full-sized cells were recently introduced in the market in order to reduce interconnection losses and therefore improving the CTM. Since this technology requires an additional process step for cutting the cells, as well as a modification of the stringer equipment, it has an impact module manufacturing process.

As shown in Fig. 46, it is expected that the market share of half cells will grow from 5% in 2018 to nearly 40% in 2028. In addition, we expect the appearance modules with quarter cells.

Fig. 47 shows that the module market splits into two main sizes: 60-cell and 72-cell modules. 96-cell modules are for special markets. The larger module sizes are mainly used in utility applications. Other module sizes for niche markets (e.g. 48 and 80 cells) are expected to account for 2% of the market during the next years. Today's mainstream modules (60-cells) will have a market share of about 35% in 2028.

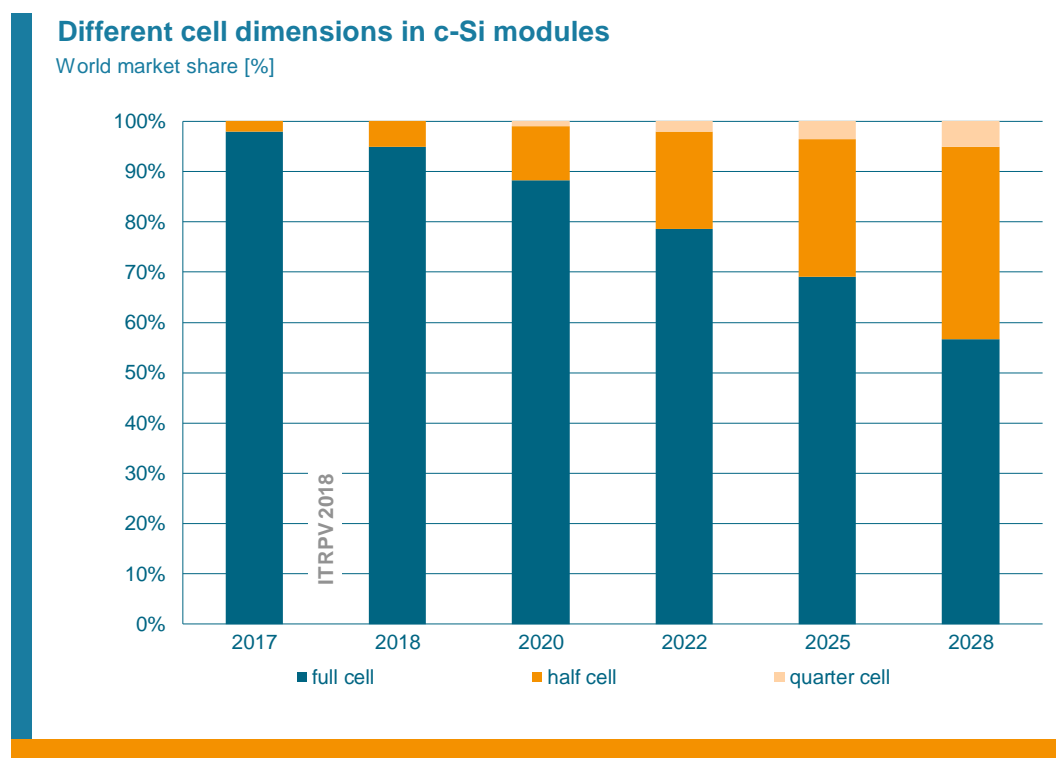


Fig. 46: Predicted market shares for modules with full, half, and quarter cells.

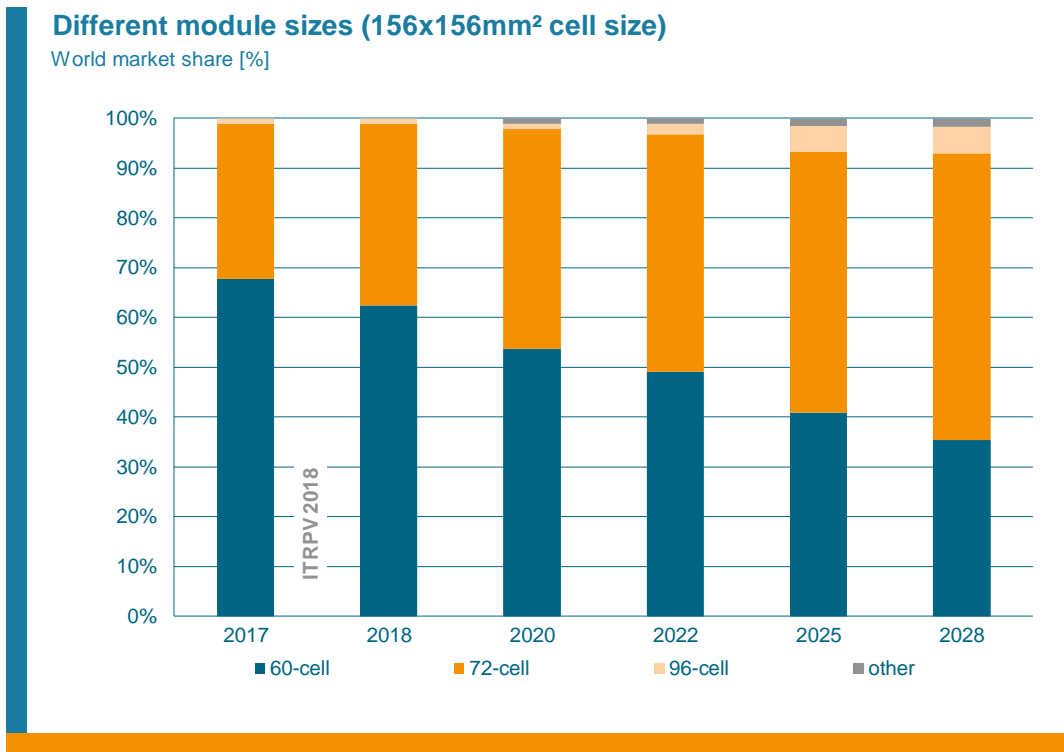


Fig. 47: Market shares of different module sizes with 156 x 156 mm<sup>2</sup> cells

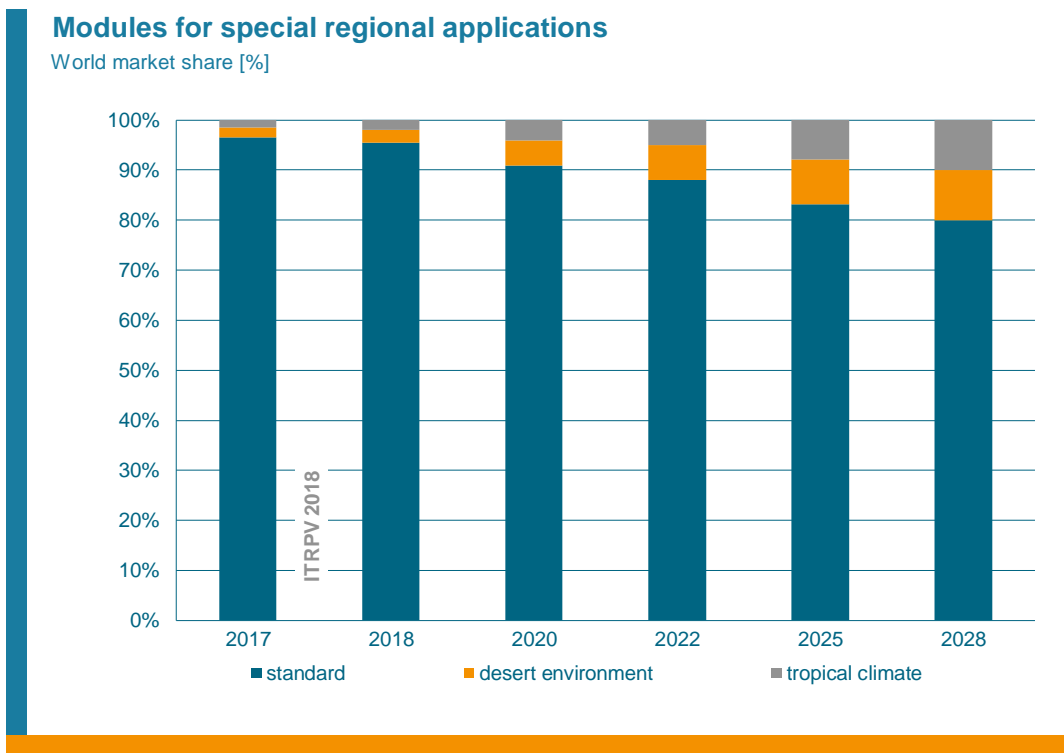


Fig. 48: Market share for special regional applications.

Another trend is the development of products for special markets and environmental conditions,

Fig. 48 shows the assumed market share of modules for special environmental conditions like for desert and for tropical climate conditions. Still in 2028 it is expected that the main market will be for standard modules and only 20% will be produced for special regions.

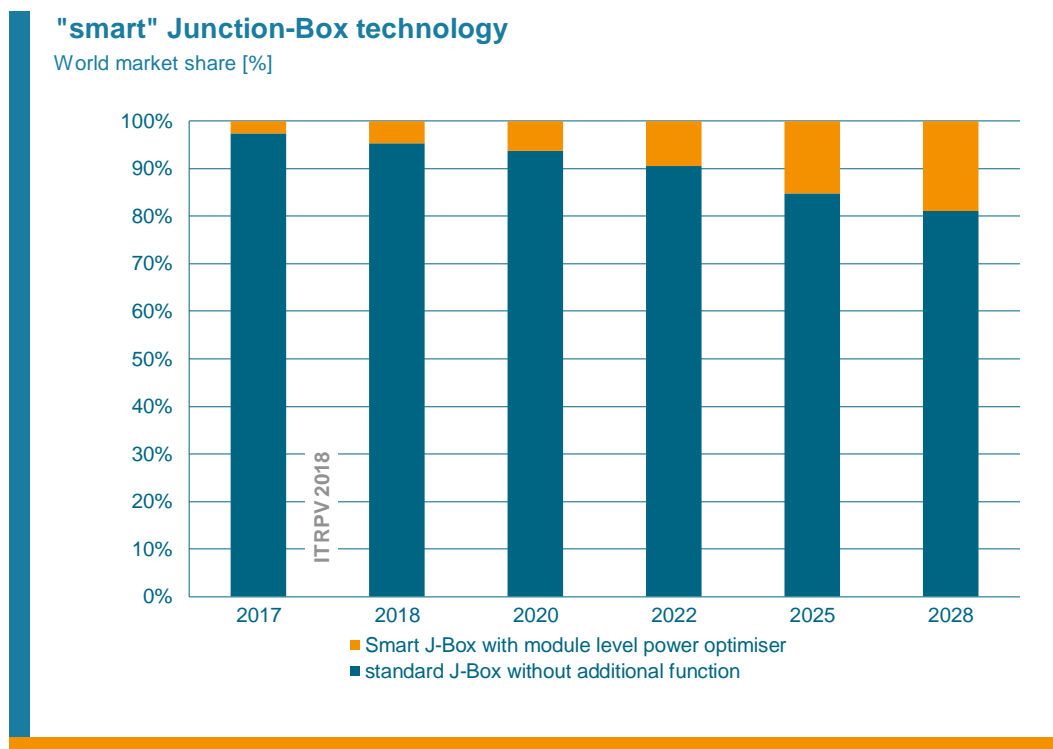


Fig. 49: Market trend for different J-Box functionalitie - smart vs. standard junction box.

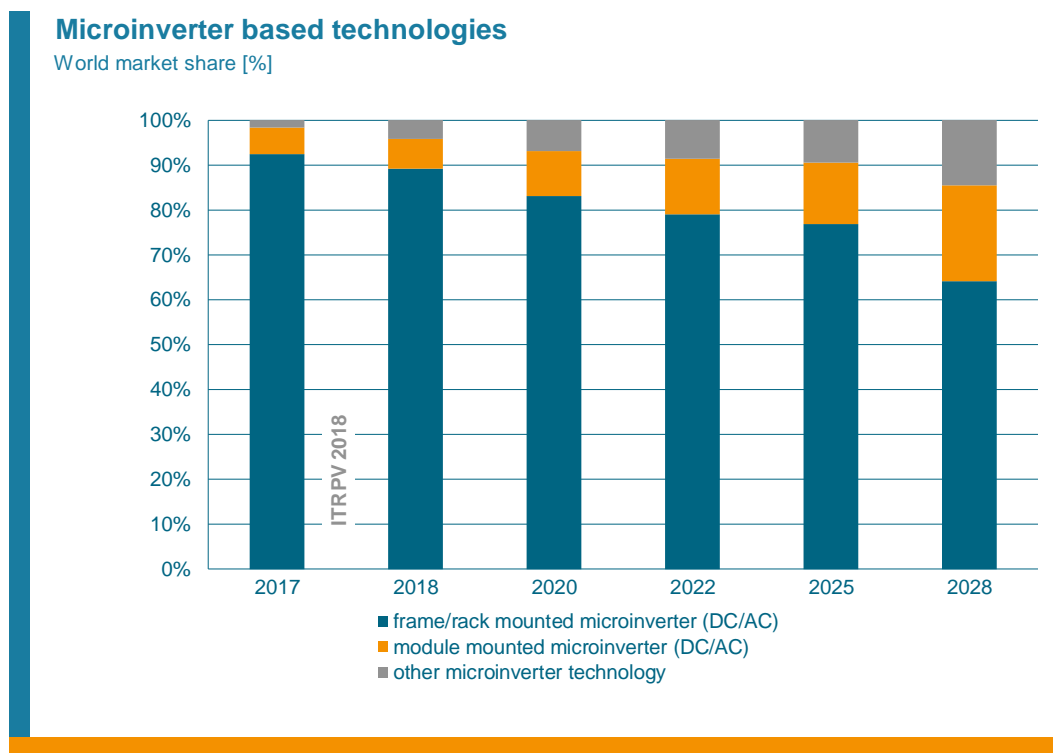


Fig. 50: Market trend for microinverter technologies (10% of the modules in 2028 are expected to include microinverters).

So-called smart J-Box technologies are anticipated to improve the power output of PV systems. As can be seen in Fig. 49, the participants in our survey believe that standard J-Box without any additional function except the bypass diodes will clearly dominate the market over the next 10 years.

DC/AC micro-inverters are expected to increase their market share to around 10% by 2028. Fig. 50 shows the expected technologies applied. Frame or rack mounted microinverters are expected to become the preferred technology in this application.

## 6. PV systems

Due to the significant reduction of PV module prices over the last few years, balance of system (BOS) costs have become a crucial factor in overall system costs and thus the levelized cost of electricity (LCOE) as well. Warranties for the product and the product performance as well as the degradation of the modules during the operation lifetime are important parameters to reduce LCOE.

Fig. 51 shows the estimated trend of these parameters for the next years. The degradation after the 1<sup>st</sup> year of operation will be reduced from currently 2.5% in in 2017/2018 to 2% from 2020 onwards. This is mainly linked to the control of light induced degradation (LID) and light and elevated temperature induced degradation (LeTID), latter especially in the case of module products with rear side passivation cell. Understanding the degradation mechanisms and a tight control of the degradation are mandatory to ensure this warranty [17]. Standards for LeTID testing are about to be developed.

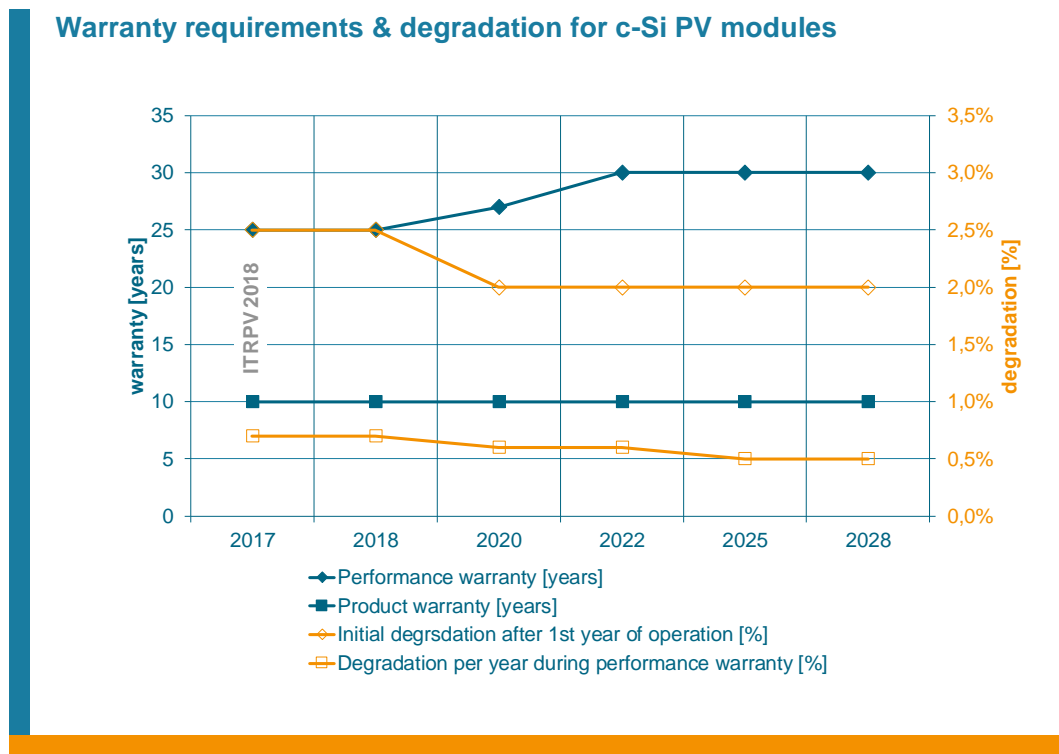


Fig. 51: Expected trend for product warranties and degradation of c-Si PV modules.



Yearly degradation is expected to be reduced slightly from 0.7% today stepwise to 0.5% over the next years. Product warranty will stay at 10 years for PV modules whereas the performance warranty is considered to increase to 30 years from 2024 onwards.

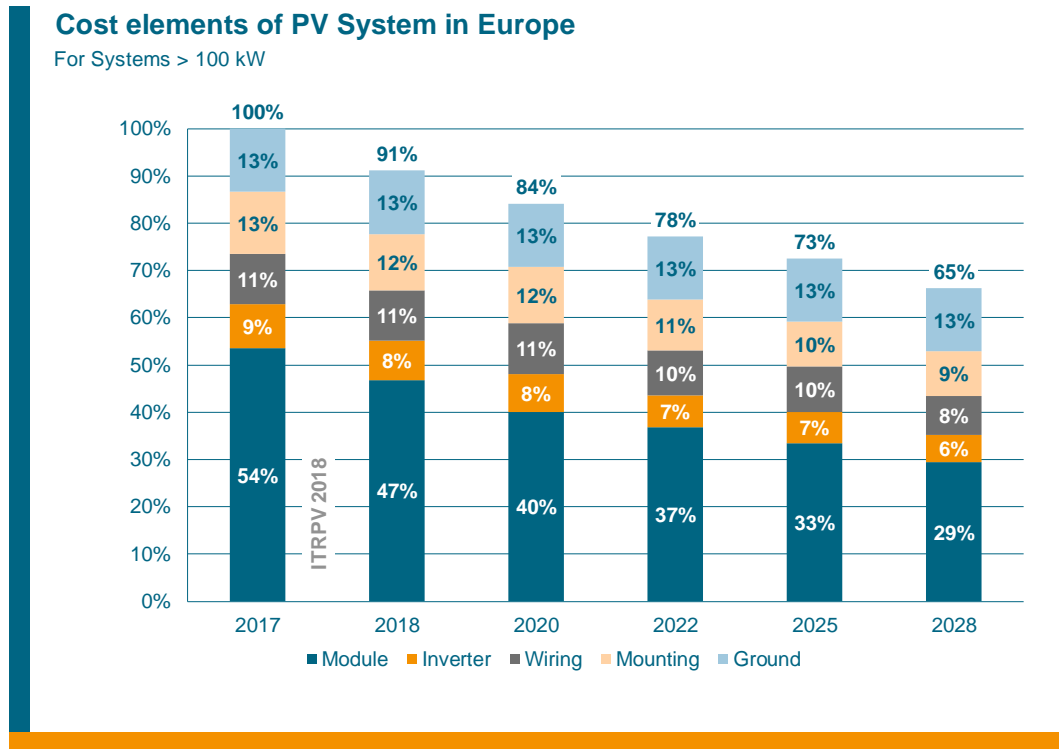


Fig. 52: Relative system cost development for systems > 100 kW in Europe (2017 = 100%)

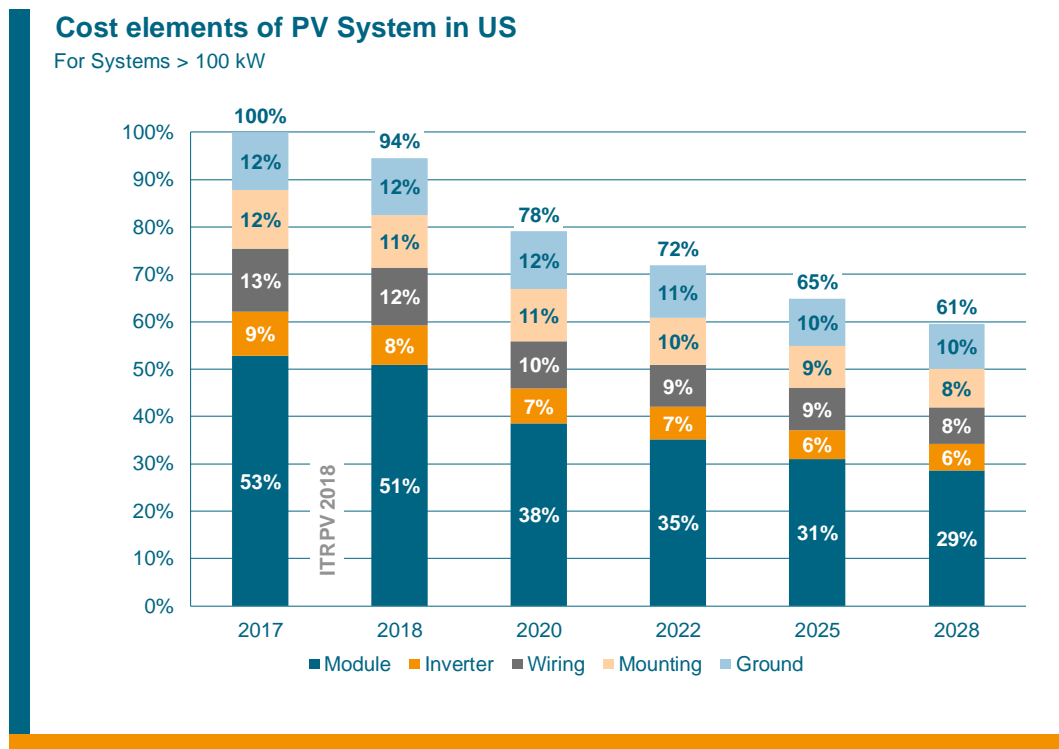


Fig. 53: Relative system cost development for systems > 100 kW in the U.S. (2017 = 100%).

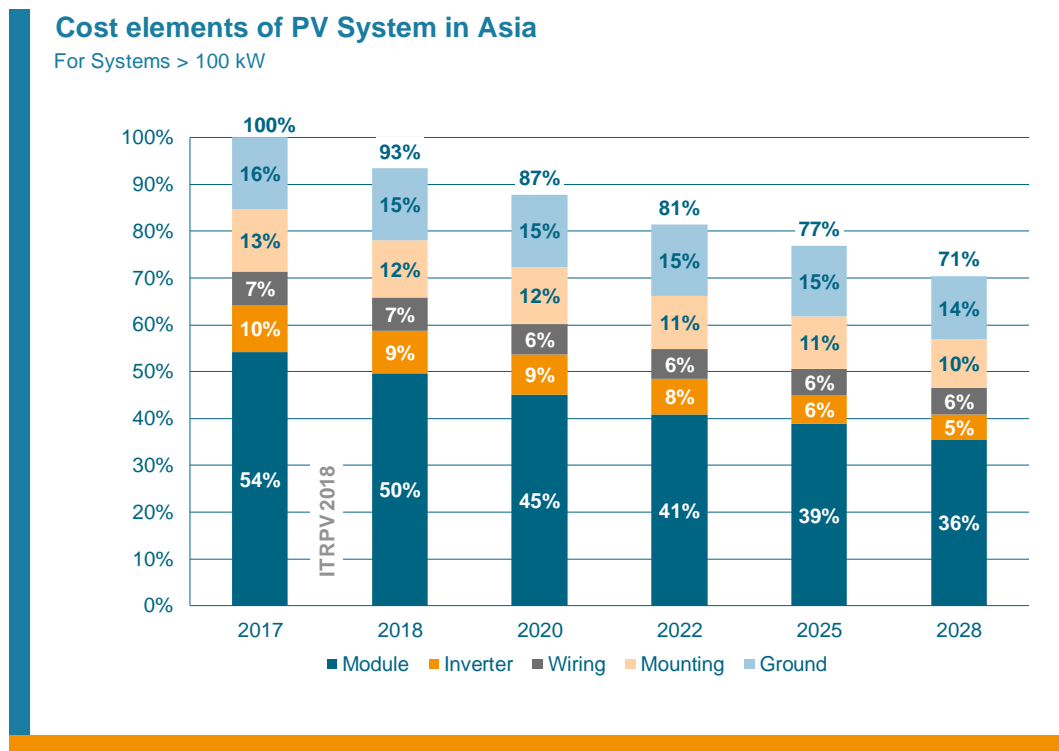


Fig. 54: Relative system cost development for systems > 100 kW in Asia (2017 = 100%).

In Figures 52, 53, and 54, the relative development of system costs for large systems >100 kWp in the U.S., Europe, and Asia is shown. It should be noted that no “soft costs,” such as costs for permits or costs for financing, are included, as these costs may vary significantly from country to country. Excluding the “soft costs,” the distribution of system costs as well as the development over time are expected to be comparable in the U.S. and Europe.

The assumptions for the US market exclude any influences on module cost due to the “Suniva” trade case.

As can be seen by comparison of Fig. 52-54, the overall trend for system cost reduction during the next ten years is expected to be similar for Asia, Europe, and the U.S. with a slightly higher decrease for Europe and U.S. Due to differences in absolute system costs, the relative distribution between the cost components of module, inverter, wiring, mounting, and ground is expected to be slightly different. The only major difference can be seen in the share of the module costs as compared to the system costs. It is expected that the module share will constantly stay higher in Asia compared to U.S. and Europe. This could possibly be explained by the lower overall system costs in Asia.

One trend to be expected on system level is the trend toward an increase of system voltage from 1,000 V to 1,500 V – from 2020 onwards the market for 1500V systems will be >30%, attaining a market share of >50% from 2025 onwards (see Fig. 55). The increase in system voltage represents an important measure for lowering resistive losses and/or BOS costs by reducing the required diameter of the connection cables within a PV system.

Furthermore, the average module power class for systems >100 kWp is expected to increase from 275 Wp in 2017 to about 350 Wp for 60-cell modules, and from 325 Wp to 395 Wp for 72-cell modules (see Fig. 56). This also should significantly support the reduction of the area-dependent BOS costs.

### Maximum system voltage of new PV systems

World market share [%]

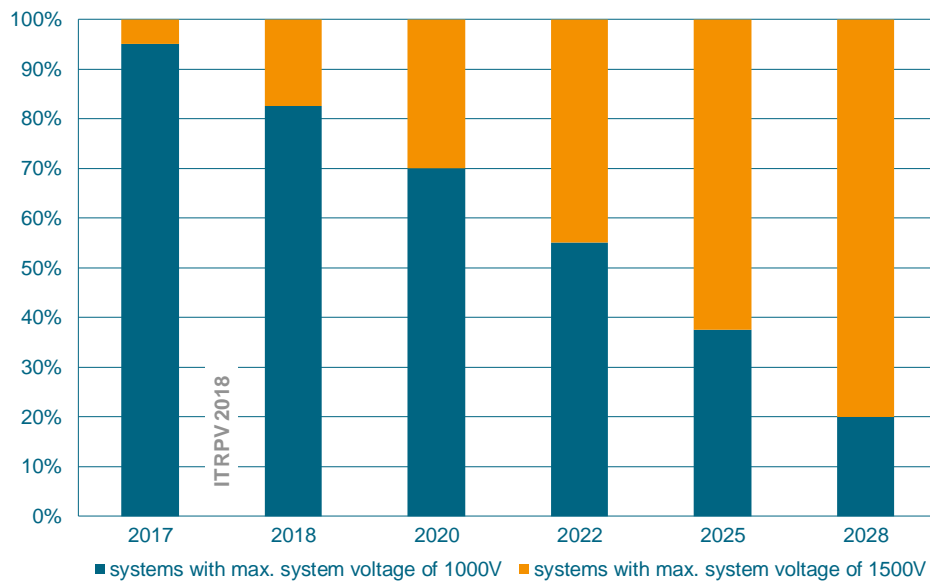


Fig. 55: Trend of maximum system voltage for systems >100kW.

### Average module power class for systems > 100 kW

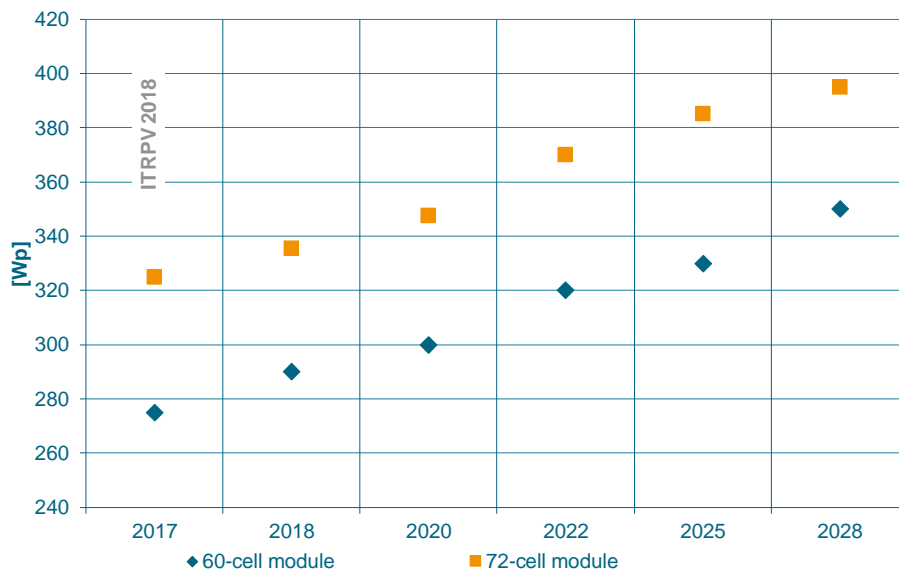


Fig. 56: Trend of average module power class for utility applications with >100kW.

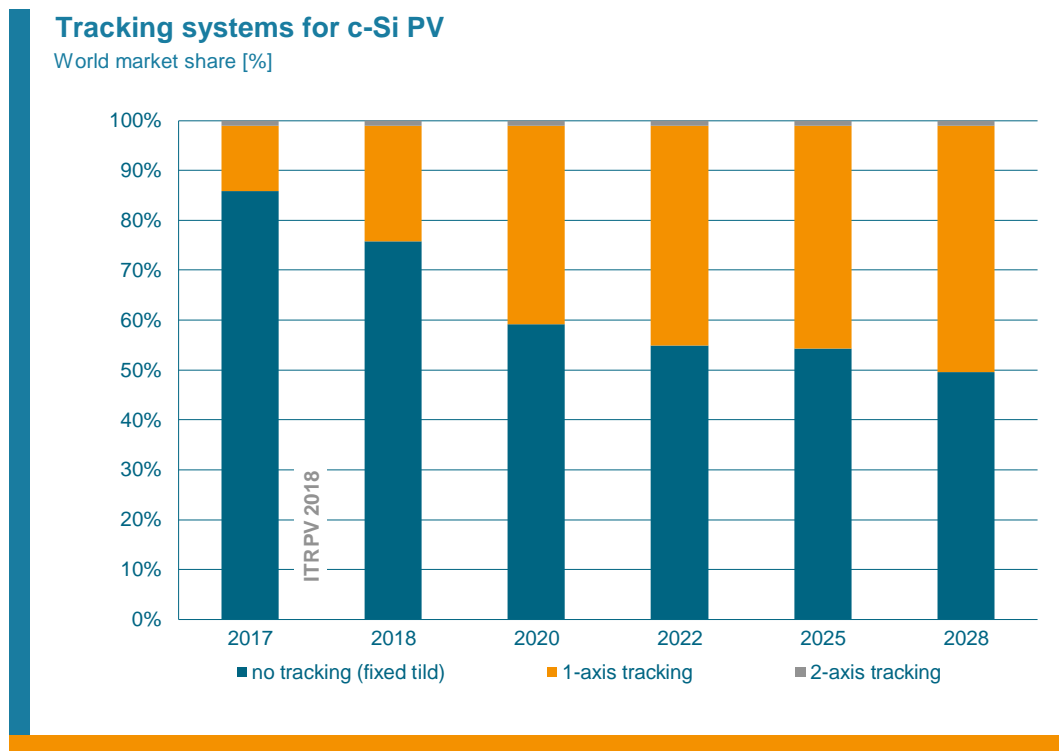


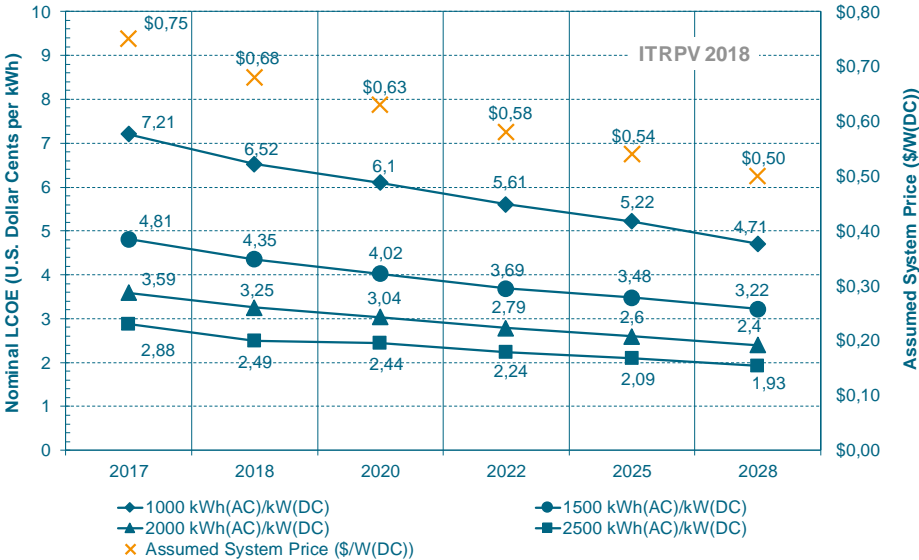
Fig. 57: Market share of tracking systems for c-Si PV installations.

Another long-term trend on the system level is again considered in the current version of the ITRPV: The market share of tracking systems in large scale c-Si based PV-systems is shown in Fig. 57. 1-axis tracking systems will increase the market share from approximately 15% in 2017 to >40% from 2020 onwards. By contrast, 2-axis tracking will remain negligible for c-Si technology with a (constant market share of around 1% during the next decade).

The levelized cost of electricity (LCOE) is a commonly recognized economic metric for comparing the relative costs of different renewable and non-renewable electricity generation technologies. To estimate 2017 benchmark and future scenarios of PV power generation costs, we have used NREL's System Advisor Model (SAM) to calculate the LCOE in USD for large PV systems deployed in different insolation conditions (see Fig. 60) [15,16]. Actual system prices and cost drivers are strongly dependent upon location. As a useful starting point, we have assumed 750 USD /kW(DC) capital costs in 2017, which would correspond to total typical module, inverter and hardware costs for PV systems having greater than 100 MW nameplate capacity in the U.S. and Europe. The so-called 'soft costs' including project developer and installer overhead and profit, and permitting, will add around another 250 USD/kW(DC) for large-scale systems in the U.S. and Europe in 2017. Project soft costs typically have the greatest variance across the globe and from project-to-project and are not included here. The system cost trends depicted in Fig. 53 assume that total direct costs will decline to around 500 USD/kW(DC) in 2028.

**LCOE Calculations For Different Insolation Conditions**

80% Debt with 18 year tenor. 20-year straight line depreciation and 25 year analysis period. 4% nominal debt and 5% nominal equity discount rates with 2% inflation.



**Fig. 58:** Calculated LCOE values for different insolation conditions. Financial conditions: 80% debt, 18-year loan tenor, 20-year straight line depreciation and 25 years usable system service life. 4%/a nominal debt rate, 5%/a nominal equity discount rate, 2%/a inflation rate. The calculations were performed using NREL’s System Advisor Model (SAM)[15].

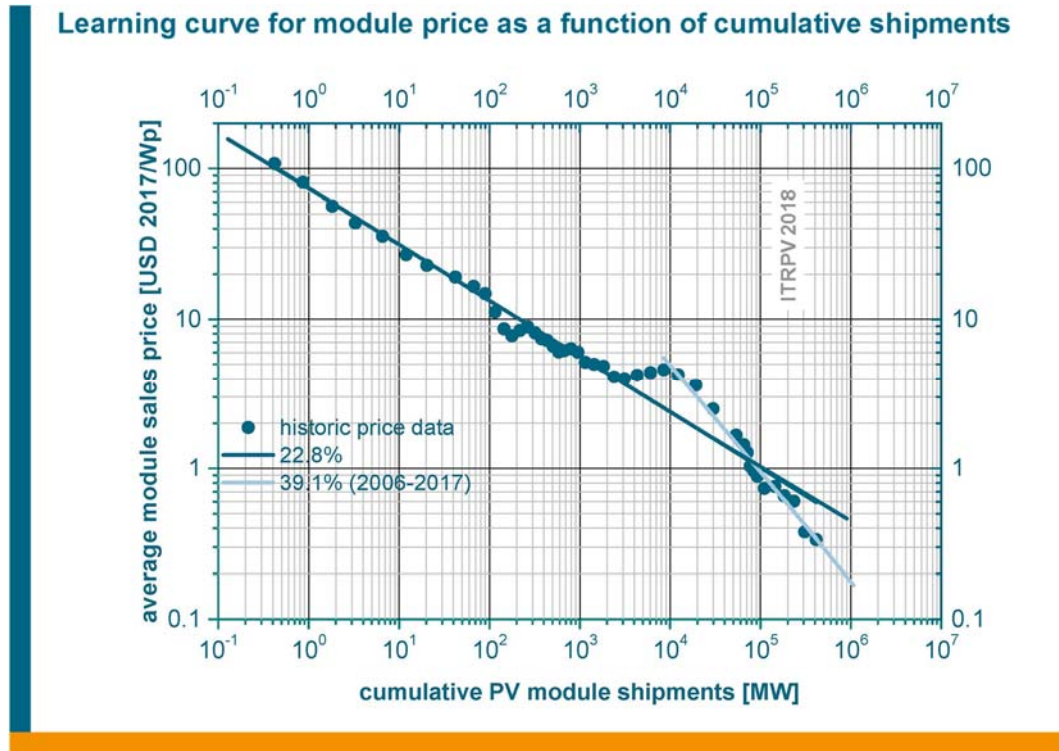
As can be seen in Fig. 58, LCOE values between 0.029 and 0.072 USD are calculated to be feasible today, depending upon the insolation level. Considering the system price trends anticipated by the ITRPV (see Fig. 52, 53, 54), PV LCOE in the range of 0.02 to 0.05 USD are predicted by the year 2028. It is important to note that, along with the system price and the insolation level, LCOE is also strongly dependent upon operations and maintenance issues, the project financing structure and the usable service life of the system. For our calculations we have assumed 25 years of usable system service life; however, it is expected that advances in module and BOS technology as outlined in the ITRPV will enable an extension of the system service life to 30 years or maybe even more. Advances in system life would make it possible to reduce LCOE levels even further. Improved financing, as a major contributor to the LCOE – due to PV becoming a lower risk electrical energy generation technology – may also allow the 2028 LCOE levels to be reached earlier. This could make PV power generation a clean, cost-competitive and valuable contributor to the world’s future energy mix. This will be discussed in the next section.

# 7. Outlook

## 7.1. PV learning curve

We discussed in Chapter 3 the current learning curve situation. Fig. 1 shows the price learning curve and the calculated price learning rate. The learning rate was calculated to be 22.8% by using all data points between 1979 and 2017. However, considering only the data points since 2006, the learning rate is 39.1% as shown in Fig. 59. 2006 was the last year of a longer period of Silicon shortage. And

2006 marks the beginning of c-Si PV mass production in China. 2006 marks the entry point into a period of continuous capacity extensions after the scarcity situation of silicon and modules during the period between 2004 and 2006.



**Fig. 59:** Learning curve of module price as a function of cumulative PV module shipments and calculated learning rates for the period 1979 to 2016 and 2006 to 2017 respectively.

Based on the above findings we started in the 8<sup>th</sup> edition the analysis about the breakdown to the two basic learning contributors – module power learning and reduction of price (cost) per piece. Table 1 summarizes average module efficiencies at different years. The price values were taken from the learning curve while module efficiencies were assumed as average module powers of p-type mc-Si and mono-Si modules of ITRPV reports (3<sup>rd</sup> to 9<sup>th</sup> edition) the module efficiency of 1980 was found in [17]. A 64% increase in module power was realized during the 30-year period from 1980 to 2010. The yearly average power learning from 2010 to 2017 was between 1% and 4% while per-piece learning varied between -9% and up to 35% for the corresponding periods.

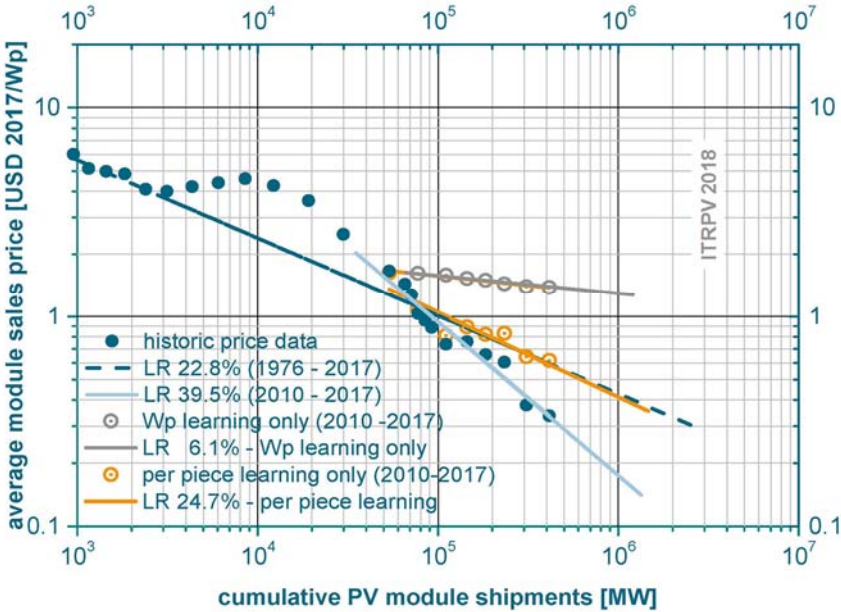
Fig. 60 shows the plot of data points for Wp learning and per piece learning according to Table 1. The calculated corresponding learning rates of 6.1% for Wp learning and 24.7% for per piece learning indicate that the main contribution of the price learning arose from per piece reductions. This is in line with the findings in [3] and emphasizes again that only the combination of Wp learning and cost reduction grants the resulting learning. Nevertheless, it can be concluded that the current price situation is not only due to cost learning but also caused by the market situation. Manufacturers are struggling with significantly reduced margins as current prices are approaching the assumed Q1 2017 pure module manufacturing costs of about 0.31\$/Wp [18].

### Year over year learning

Year	1980	2010	2011	2012	2013	2014	2015	2016	2017
avg. Module power p- type (ITRPV-data)	147.6	241.5	248	253	262	267.5	278.5	287.5	290
Module efficiency [%], avg. Mod. area: 1.64m <sup>2</sup>	9 [15]	14.7	15.1	15.4	16	16.3	17	17.5	17.7
Module price [\$2017]	35.7	1.66	1.04	0.74	0.76	0.66	0.61	0.38	0.34
Module price (Wp-increase only) [USD(2017)/Wp]		1.63	1.62	1.59	1.53	1.50	1.44	1.40	1.38
Module price (cost reduction per piece only) [USD (2017)/Wp]		1.63	1.08	0.81	0.89	0.82	0.83	0.643	0.62

**Table 1:** Yearly learning for module efficiency and price per piece based on module price data (2010 = 100%) [4, 5, 6], module efficiencies calculated from ITRPV module power values (3<sup>rd</sup> to 9<sup>th</sup> edition); 1980 module power is calculated from efficiency in [17].

### Learning curve for module price as a function of cumulative shipments



**Fig. 60:** Learning curve of module price as a function of cumulative PV module shipments, update on calculated learning rates for the period 1979 to 2017 and 2006 to 2017 respectively, calculated Wp and per piece learning including learning rates according to Table 1.

### 7.2. PV market development considerations

The most widely publicly discussed PV-related topics and trends are installed PV module power, module shipments, as well as scenarios about the PV generated electricity. A look at the supplier side, to follow the market development of PV modules, cells, wafers and polysilicon, is less spectacular, but it is essential for investment planning. The analysis of the annual PV market development until 2050 was started in the ITRPV 6<sup>th</sup> edition. In the following section, analyses of previous ITRPV editions are

compared in view of 2017 PV installation results. One scenario of the 7<sup>th</sup> edition and two PV installation scenarios of the 8<sup>th</sup> edition, detailed on a country-by-country base for more than 190 countries in four regions (Americas, Africa, Europe, and Asia), will be discussed below.

The IEA developed three scenarios for the energy consumption and generation until 2050, based on assumptions about population growth and energy consumption behavior [19]. The most optimistic scenario considers the limitation of global temperature increase to 2°C at the end of the 21<sup>st</sup> century. This scenario assumes the highest amount of PV generated electricity - sufficient to cover 16% of global electricity demand in 2050. Due to the expected competitiveness of PV, this scenario can be considered as “Low Scenario”. A slightly more ambitious scenario, assuming a limitation of global temperature increase to 1.75°C with even higher requirements on PV deployment is discussed in [20]. The “High Scenario” includes contributions to the primary energy consumption by PV on top of providing electricity only. This scenario includes a conservative wear out period of only 25 years. Power generation yield is calculated for each country in detail varying from 800 kWh/kWp in low insolation countries and >1700 kWh/kWp in high insolation countries [21]. As third scenario we consider an even more ambitious 2<sup>nd</sup> scenario of the 7<sup>th</sup> edition of the ITRPV, calculated not on a country by country approach but on a regional assumption only as described in [22].

Based on the assumptions in we calculated the scenarios below:

1. Low Scenario: 4.5 TWp of installed PV in 2050, generating 7.05 PWh
2. High Scenario: 9.17 TWp of installed PV in 2050, generating 14.3 PWh
3. Mix Scenario: 23 TWp of installed PV in 2050+ generating 30.0 PWh

Using these figures and deducting the annual installed PV power  $P_{PV}(t)$  as the sum of the installed PV power of  $j$  different regions  $N_i(t)$  was calculated to be:

$$P_{PV}(t) = \sum_{i=1}^j N_i(t)$$

The installed module power in each region  $N_i(t)$  was calculated as the sum of the installed power of  $m$  individual countries belonging to one of the four regions  $l$ ,  $L_{li}(t)$ :

$$N_i(t) = \sum_{l=1}^m L_{li}(t)$$

Using the logarithmic growth approach, where  $K_{li}$  is the maximum installed PV power in the market of the considered country (or asymptote),  $Q_{li}$  is a scaling parameter,  $B_{li}$  is the growth slope, and  $M_{li}$  is the time constant for the country in question an  $v_{li}$  asymptote factor:

$$L_{li}(t) = \frac{K_{li}}{(1 + Q_{li}e^{B_{li}(M_{li}-t)})^{1/v_{li}}}$$

The global annual addressable market of year  $n$   $AM(n)$  corresponds to the installed module power in year  $n$ . It was calculated by subtracting  $P_{PV}(n-1)$  from  $P_{PV}(n)$  plus adding the replacement volume of the worn-out installations  $P_{PV}(n-25)$ . For this approach, a conservative wear-out period of 25 years was assumed.

$$AM(n) = P_{PV}(n) - P_{PV}(n-1) + P_{PV}(n-25)$$



The model defines for the individual countries an individual set of growth parameters for each of the mentioned scenarios. As example, we summarize in Table 2 scenario 3 parameter sets of four countries contributing to the four regions:

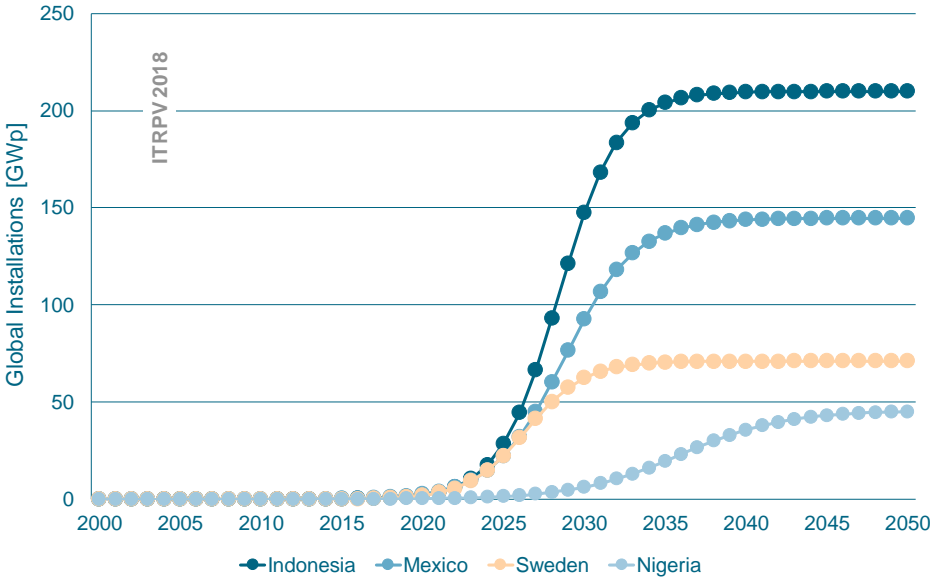
**Logistic growth parameter for four countries in the High Scenario**

	Country	$K_{ij}$ (PV power 2050)	$Q_{ij}$ (scaling factor)	$B_{ij}$ (growth slope)	$M_{ij}$ (time of max growth)	$V_{ij}$ (asymptote factor)
<b>Africa</b>	Nigeria	45.67 GW	10.63	0.04	2028	0.14
<b>Americas</b>	Mexico	144.60 GW	7.50	0.02	2024	0.05
<b>Asia</b>	Indonesia	209.83 GW	0.73	0.28	2029	0.51
<b>Europe</b>	Sweden	71.01 GW	5.50	0.27	2023	0,49

**Table 2:** Logistic growth parameter for four different countries in the High Scenario.

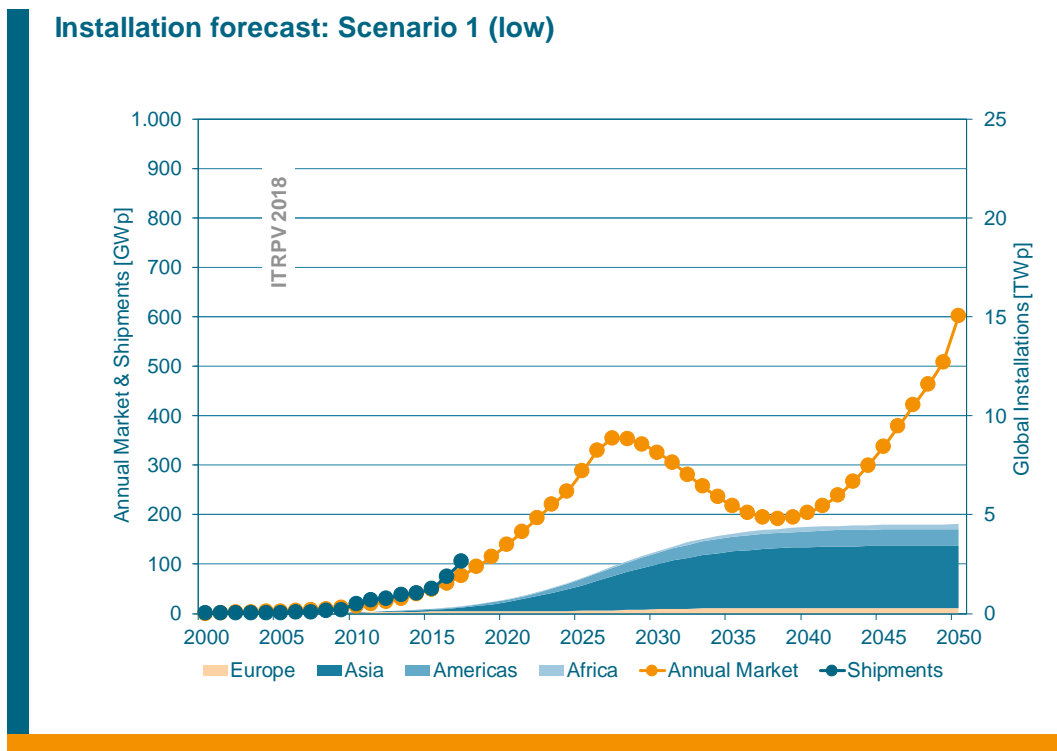
Fig. 61 shows the resulting cumulated installed PV power of the Nigeria, Mexico, Indonesia, and Sweden for scenario 2 – the high scenario, calculated with the parameters listed in Tab. 2

**Installation forecast: Scenario 2 (high)**



**Fig. 61:** Calculated cumulated installed PV power of 4 different countries for scenario 2 – high scenario.

Fig. 62 to 64 show for all scenarios the plots of the cumulated installations, the annual market, and historic PV shipment data (until 2017).



**Fig. 62:** Cumulative installed PV module power and annual market calculated with a logistic growth approximation for Scenario 1, assuming 4.5TWp installed PV module power in 2050.

Fig. 62 shows scenario 1, the Low scenario, in line with IEA expectations [19]. The addressable PV market and the corresponding production capacity would require an expansion to 200 GWp until 2022 with a peak of 355 GWp in 2027. After this peak, demand is calculated to decline again to about 200 GWp between 2035 and 2040. This up-and-down development will repeat due to the replacement of old systems after 25 years of operation. This fact emphasizes the importance of PV-module reliability; as longer module lifetime will help to realize this development to some extent.

Fig 63 shows the scenario 2 – high scenario. In this case, the addressable PV market and the corresponding production capacity would rapidly expand to a peak of around 660 GWp per year in 2030. A repeated up-and-down development would appear as well due to the 25 years replacement cycle. The annual market growth is calculated to about 60GW per year around 2025.

Scenario 3, the mix scenario, is summarized in table 3. It was calculated according to the parameters discussed in the 7<sup>th</sup> editions.

Installation forecast: Scenario 2 (high)

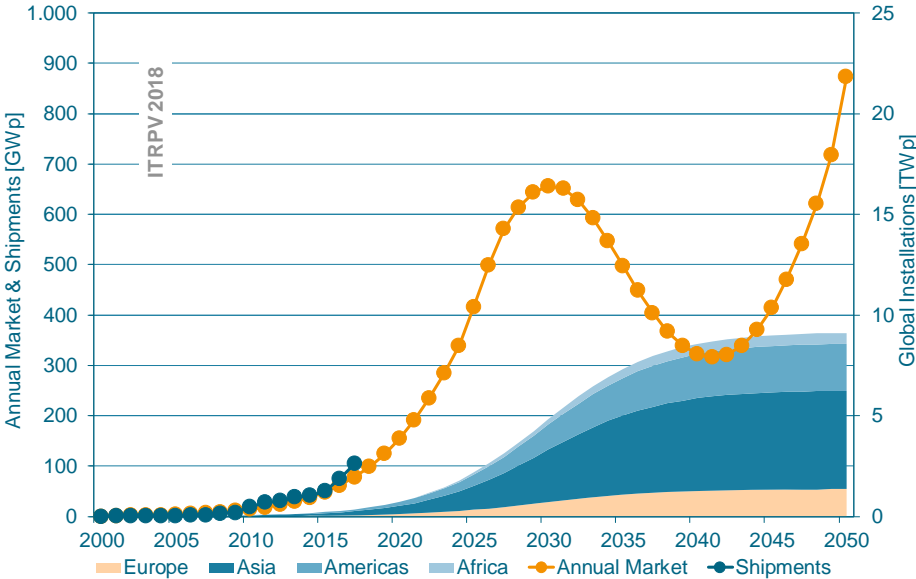


Fig. 63: Cumulative installed PV module power and annual market calculated with a logistic growth approximation for Scenario 2 – high scenario, assuming 9.17 TWp installed PV module power in 2050.

The installed module power in each region  $N_i$  was calculated using the logistic growth approach in which  $G_i$  is the maximum installed power in the market,  $k_i$  is the growth slope and  $c_i$  is the time constant for the market in question:

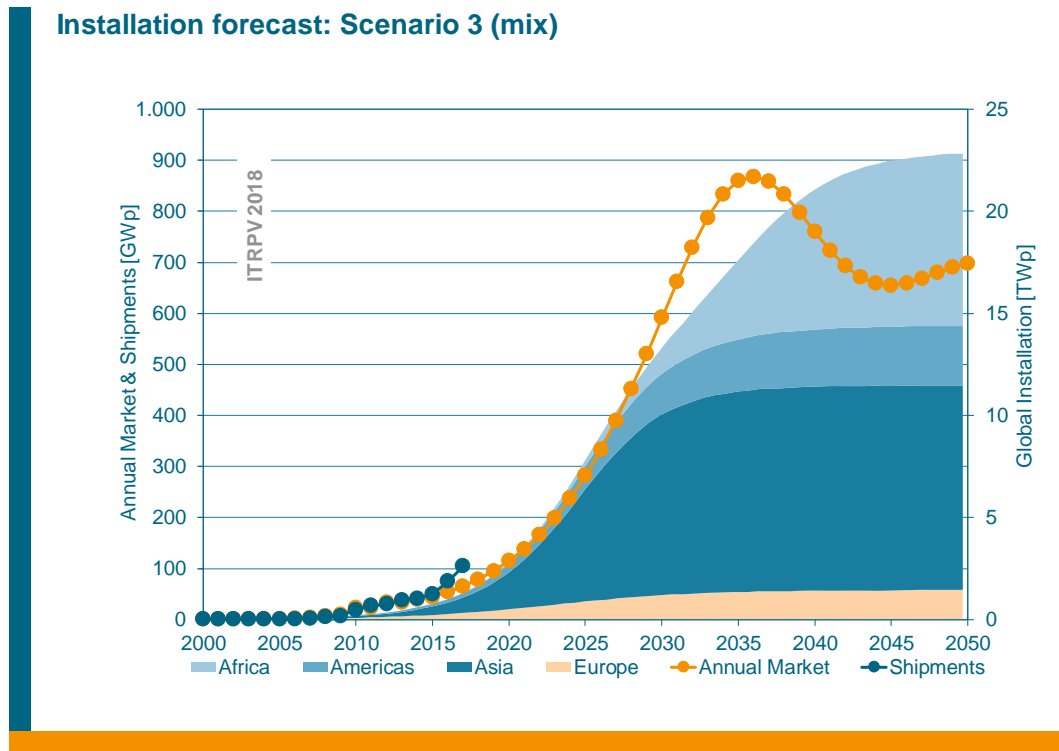
$$N_i(t) = \frac{G_i}{1 + e^{k_i(c_i-t)}}$$

Logistic growth parameter of key regions

Region	Sub-region	$G_i$ (PV power in 2050+)	$k_i$ (growth slope)	$c_i$ (time constant)
<b>Africa</b>		8600 GW	0.22	2050
<b>Asia</b>	PR China	2000 GW	0.22	2030
	India	3100 GW	0.25	2035
	Asian countries	4900 GW	0.28	2035
<b>Americas</b>	North America	1200 GW	0.20	2035
	Latin America	1700 GW	0.17	2040
<b>Europe</b>		1500GW	0.15	2032

Table 3: Logistic growth parameters of key regions according to the mixed scenario with a simplified sub-regional consideration according to [22]

The result is shown in Fig. 64. In this scenario, the addressable PV market and the corresponding production capacity would expand to around 880 GWp around 2035. Growth rate around 2025 would be between 60 and 70 GWp per year in this scenario.



**Fig. 64:** Cumulative installed PV module power and annual market calculated with a logistic growth approximation for Scenario 3 – mix scenario, assuming 23 TWp installed PV module power in 2050.

Cycles due to module lifetime of 30 years – in this case - will also occur. The intensity of the cycling may also be softened by considering changes in replacements and improved module life times.

We find in all three scenarios that the current shipment data are well above the predicted market data! On top we have to state that, again, also very optimistic scenarios were outperformed by the current shipment situation.

All three scenarios show that there will be a considerable module market in the future – with the experience of last year’s market growth by about 30GW - we may consider also higher growth scenarios as manageable. Nevertheless, there is a risk of overheated market present especially as production capacity is currently exceeding the shipments by about 30% as discussed in 1.

The considerations show that, also for different growth scenarios, there will neither be an “endless” market for PV modules, nor will there be “endless” production capacity increase needed. However, there will be on the long run a large market with possible critical demand peaks. Failing to manage the growth will lead to overheated markets with subsequent production overcapacities and shake-outs similar to the period the PV industry faced in 2012 and 2016.

Beside the expected increase of PV installation and production, recycling needs will become more important in the future – both as business opportunity and as challenge [23].

Progressive tool concepts in cell manufacturing for production lines with matched throughput between front and back end, as discussed in Section 5, will support future production capacity increase.

Anyhow, a further increase of production above a 500 GWp level will require new and lower cost production technologies.

PV equipment suppliers have currently to support upgrades of existing production capacities for new technologies such as PERC and the installation of new production capacities. New c-Si capacities will be implemented mostly for the maturing PERC concepts but also for n-type HJT technologies. The continued support of depreciated production lines, the replacement of worn-out equipment and the support of upcoming capacity expansions will constitute a considerable business segment in the future. All of this continues the positive outlook for the whole c-Si PV industry.

All activities for increasing module power and cell efficiency, ensuring more efficient wafering and poly-Si usage, and achieving a higher utilization of production capacities as discussed in the current ITRPV edition will help manufacturers in their efforts to supply the market with highly competitive and reliable c-Si PV power generation products in the years to come.

### 7.3. Accuracy of roadmap projections

ITRPV has been publishing reports since 2010. Since the first edition, the investigated parameters have been reported as median values of the past year as well as predictions for the current year and the next 10 years to come. The data of the first reported year are therefore state of the art values of technical parameters and status quo values for others. In [24] we reviewed for the first time the forecast quality of several technical parameters like the amount of remaining silver of a 156 x 156 mm<sup>2</sup> c-Si cell and the as-cut wafer thickness of c-Si wafers.

Fig. 65a, 65b and Fig. 66 show the data of all ITRPV reports for remaining silver per cell / front side finger width and for the sheet resistance.

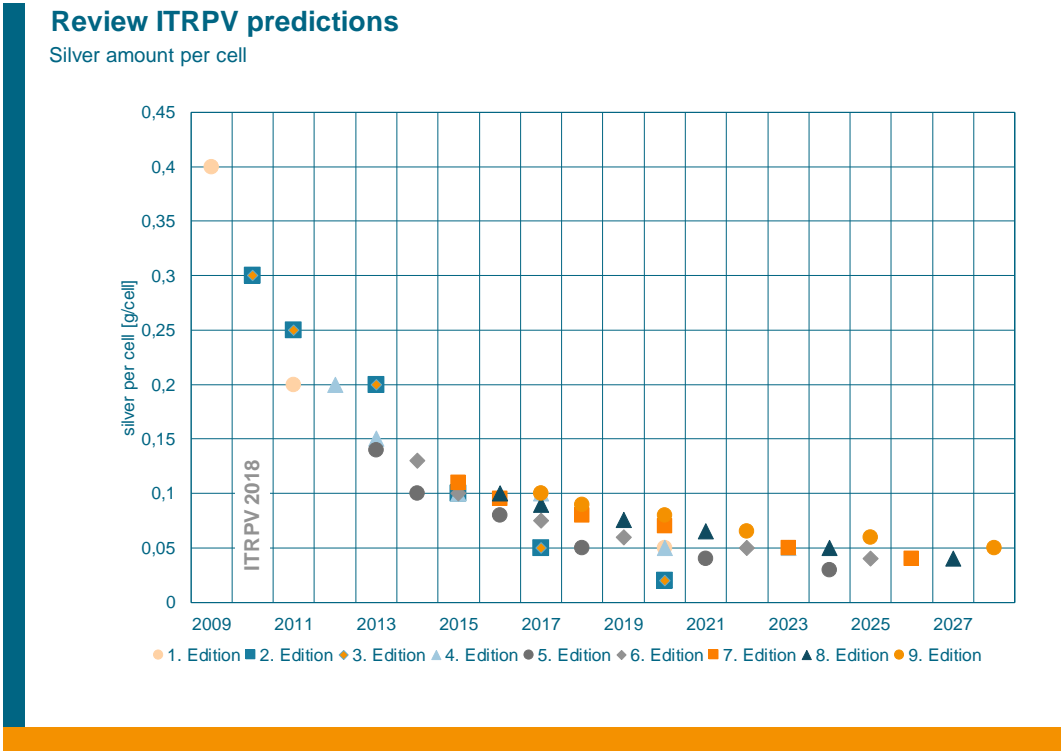


Fig. 65a: Predicted trend for remaining silver per cell (156 x 156mm<sup>2</sup>) - predictions of ITRPV editions.

Fig. 65a shows that Silver reduction – including the data of the 9th edition - has been predicted quite well since the first edition.

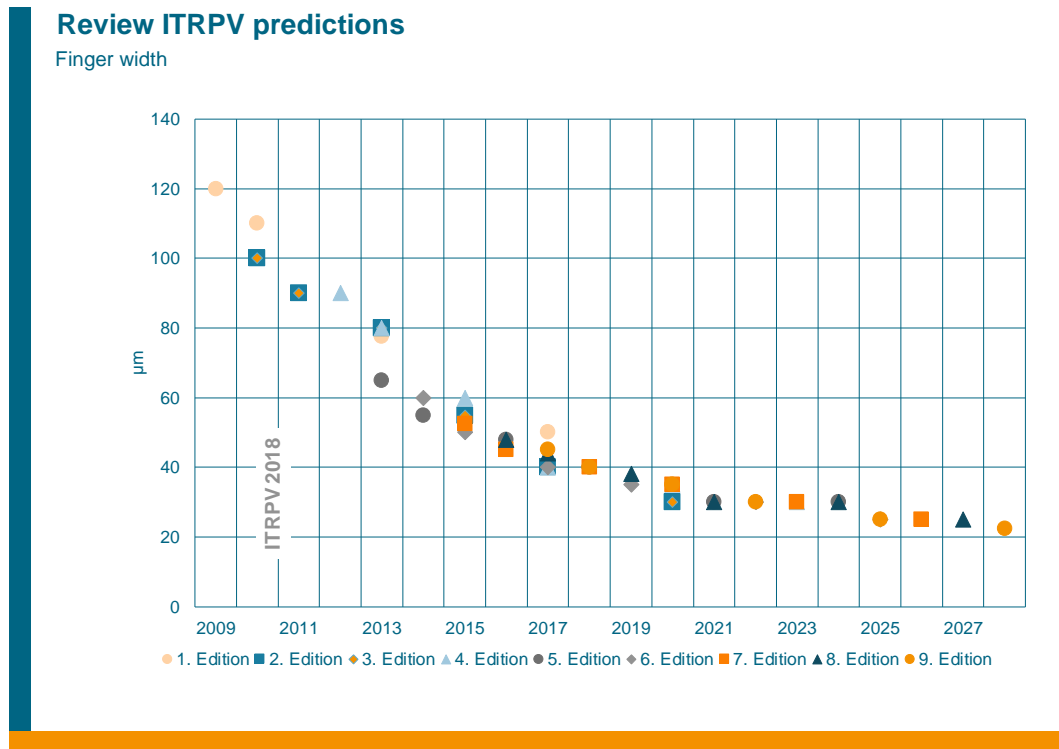


Fig. 65b: Predicted trend of finger width at front side print – predictions of ITRPV editions.

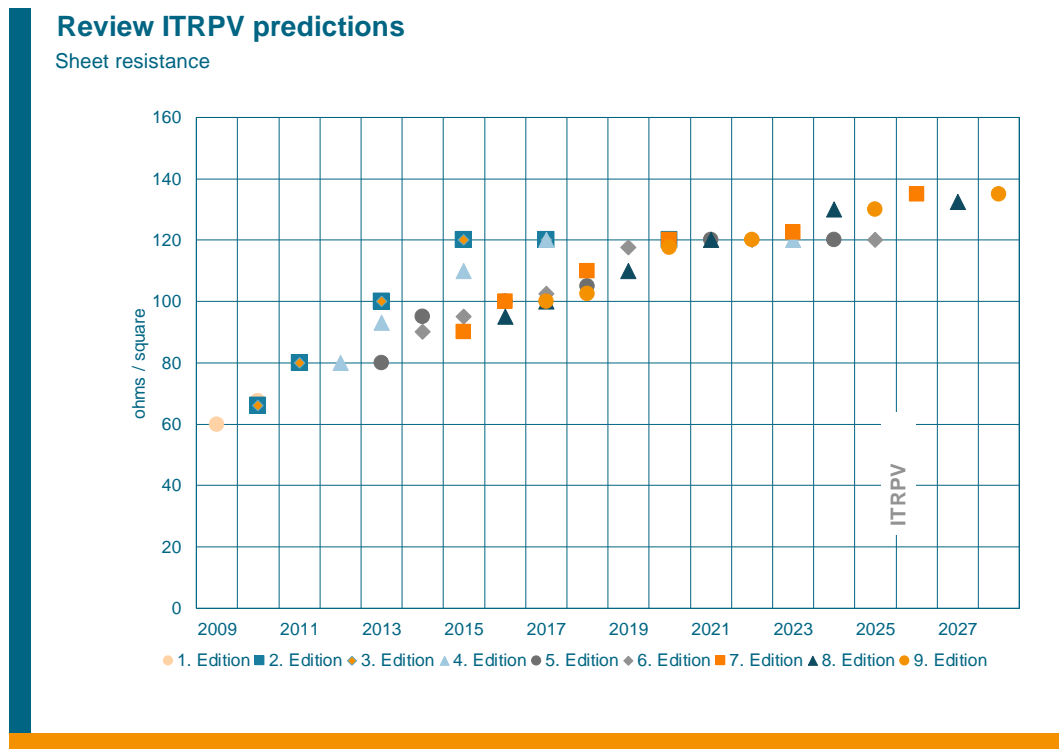


Fig. 66: Predicted trend of emitter sheet resistance of for p-type Phosphorous doped emitters – predictions of ITRPV editions.

This reveals that the initial cost saving activities have been consistently continued. This is reasonable as Silver is still the costliest non-silicon material in the c-Si PV value chain and a resource used not only by PV but also by other industries. The dependency on the world market requires continues reduction of silver consumption. Reduced usage of Silver will be mandatory to stay competitive.

The emitter sheet resistance was continuously reduced during the past. This is impressively in line with the ITRPV predictions as visualized in Fig 66.

Fig. 67a and 67b visualize the prediction quality regarding reduction of wafer thickness for mc-Si and mono Si wafers. The expected predictions could not be met at all. In contrast to Silver, Si is a material mainly produced and used in PV (beside in microelectronics).

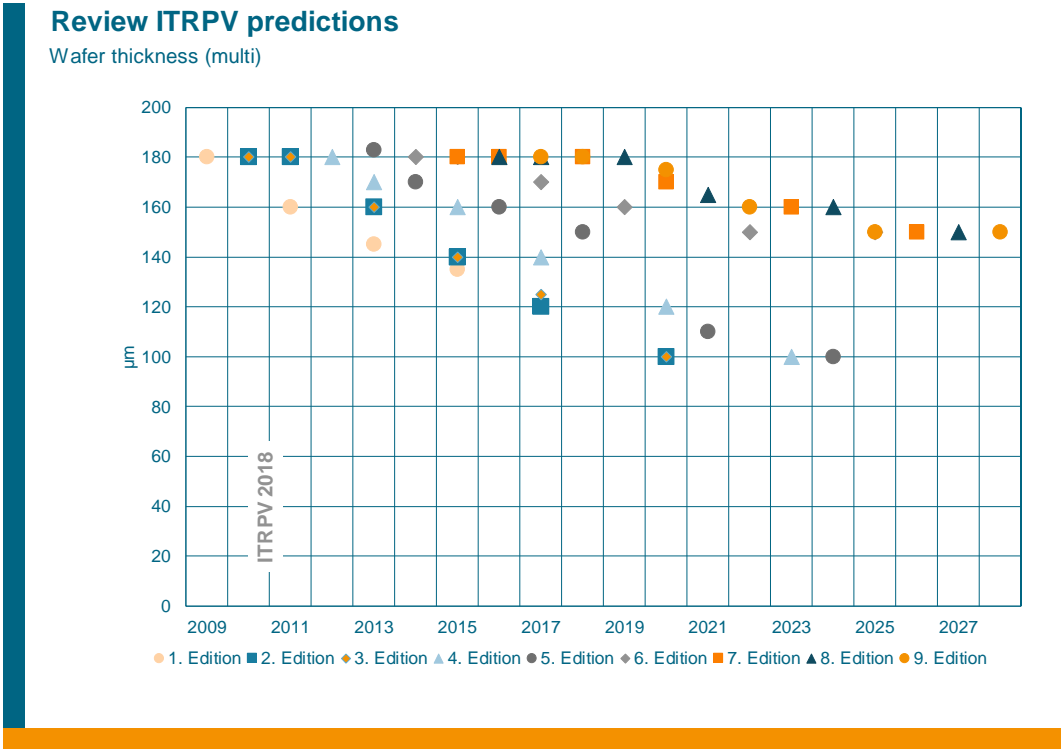


Fig. 67a: Predicted trend for minimum as-cut wafer thickness for c-Si solar cells - predictions of ITRPV editions.

Capacity increases and corresponding price reductions for poly-Si slowed down ambitious activities for material reduction. With continued cost pressure, thickness reduction will materialize – for mono-Si we see a first indication that thickness reductions will materialize.

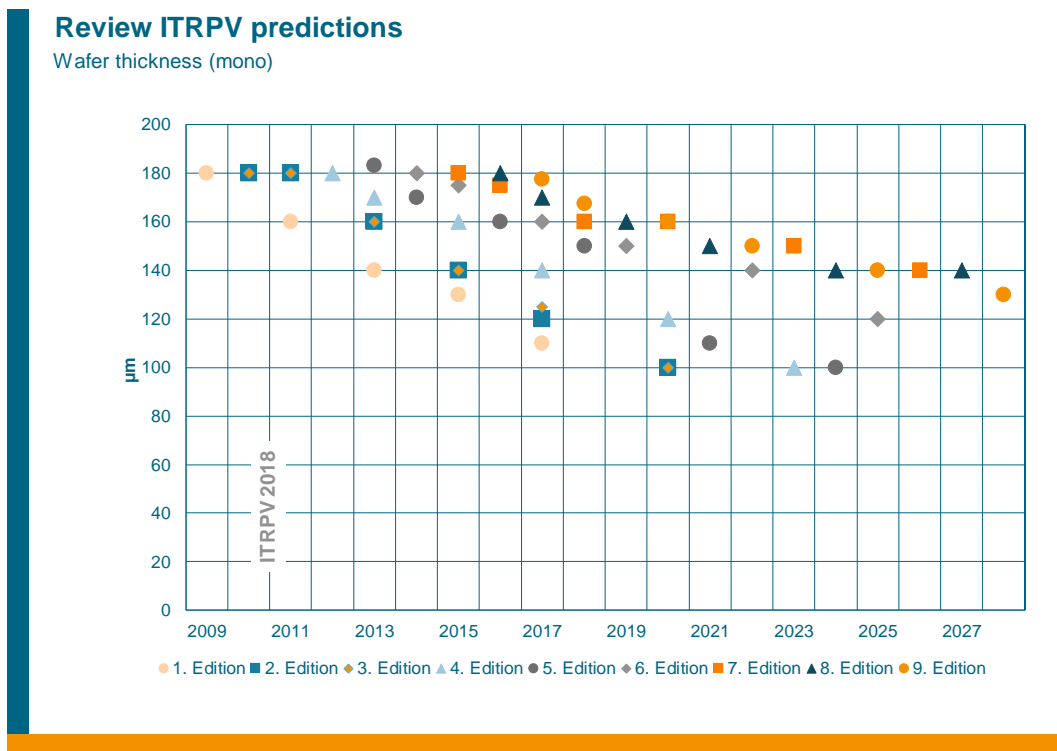


Fig. 67b: Predicted trend for minimum as-cut wafer thickness for c-Si solar cells - predictions of ITRPV editions.

#### 7.4. Projection accuracy and deviations (by P. Baliozian Fraunhofer ISE)

ITRPV was first introduced in 2010 and evolves yearly to include a larger number of projected parameters. The investigated parameters are reported as median values of the past year as well as predictions for the current year and the 10 following years. An essential phase of technology roadmapping is the follow-up process, which includes the critique and validation of the roadmap [25]. As part of the follow-up process, a parameter based accuracy study is also beneficial to further understand the deviations in previous projections. The projection quality of some parameters is first discussed in Ref [24], where the plots of the different editions are superimposed, thus showing the projection trend in each edition. To further quantify the accuracy of projections, Ref [26] proposes projection deviation statistical measures such as the projection absolute deviation (*PAD*) and the projection absolute percentage deviation (*PAPD*) to further quantify the time-dependent deviations.

The projection absolute deviation is described by the equation:

$$PAD = |P - Y|$$

*P* is the projected value of the parameter in a previous report of a certain year and *Y* is the reference value taken to be the latest report value of the result year (for instance, this year's reference value is the 9<sup>th</sup> edition values of 2017). The latest 9<sup>th</sup> edition result is taken as a reference value for the deviation calculations considering it the closest to the current market value.

The projection absolute percentage deviation is described by equation:

$$PAPD = PAD/Y * 100$$

The dependency of the projection deviation on the time span of the projection is shown in Fig. 68 where the projection absolute percentage deviation of the three parameter: silver amount per cell,



finger width, and mc-Si wafer thickness is plotted. It becomes obvious from the given data that the *PAPD* is strongly parameter and time dependent.

The line in the plot shows the time-dependent projection deviation trend deduced in Ref [26], where six parameters were studied. The general trend shows an expected decrease in the deviation with the decrease in the projection time-span, meaning that the closer the projection to the reference the less is the deviation, overall a linear approach fits to the general trend of the analysed data. As an example of an exception to the trend, the 4<sup>th</sup> edition predicted the current value of the silver amount per cell more accurately than the 5<sup>th</sup> edition.

Having a time-dependent percentage deviation value for each parameter learned from previous reports allow not only to judge the accuracy of individual reports but also to anticipate future ranges of expected results. In other words, the uncertainty or inaccuracy of the future results can be foreseen from data taken from past editions. In the future, including further parameters can provide a holistic projection accuracy analysis of ITRPV.

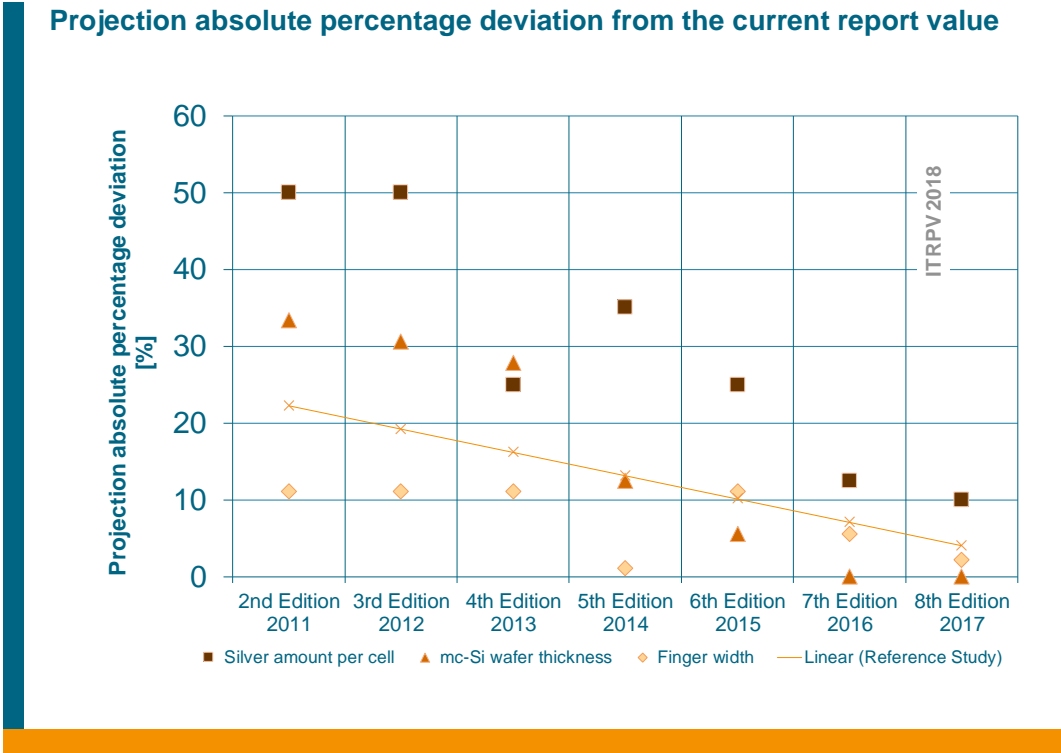


Fig. 68: The projection absolute percentage deviation from the 9<sup>th</sup> Edition 2017 values of the three chosen parameters: silver amount per cell, mc-Si wafer thickness, and finger width. The time-dependency linear trend taken from Ref [24] considers six studied parameters and shows the improvement of the projection the closer it is to the reference year.

### 7.5. Final remarks

We collected all data presented in this roadmap at the end of 2017 from leading international PV manufacturers, companies along the c-Si value chain, PV equipment suppliers, production material providers, PV institutes and PV service providers listed in the Acknowledgment. Plans call for this information to be updated annually. The topics discussed require cooperation between tool and material suppliers, manufacturers, and other companies along the value chain. A version of this document

for download, as well as information on how to get involved in roadmap activities, can be found at the following website: [www.itrpv.net](http://www.itrpv.net).

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### 9.1. Contributors and authors

Narahari S Pujari, **Alpha Assembly Solutions**  
 Giorgio Cellere, **Applied Materials**  
 Tom Falcon, **ASM Alternative Energy**  
 Martijn Zwegers, **Meco (BE Semiconductor Industries)**  
 Johannes Bernreuter, **Bernreuter Research**  
 Josef Haase, **centrotherm international AG**  
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 Christopher Berge, **ISRA VISION**  
 Qi Wang\*, **Jinko Solar**  
 Bruce W. Lee, Donald Cullen, **MacDermid Enthone Electronics Solutions**  
 André Richter, **Meyer Burger**  
 Iñaki Legarda-Ereño, **Mondragon Assembly**  
 Chi-Chun Li\*, **Motech Industries**  
 Hannes Rostan, **Mundra Solar PV**  
 Michael Woodhouse\*, **National Renewable Energy Laboratory**  
 Alex Hsu\*, **Neo Solar Power**  
 Stefan Reber, **NexWafe**  
 Christopher Case, **Oxford PV**  
 Oliver Anspach, **PV Crystalox Solar Silicon**  
 Wolfgang Jooß, **RCT Solutions**  
 Shankar G. Sridhara, **REC Group**  
 Stein Julsrud\*, Kirt Johnson, **REC Silicon**  
 Ulrich Jäger, **RENA Technologies**  
 Michael Essich, **Robert BÜRKLE**  
 Dongil Shin, **Samsung SDI**  
 Tony Chang\*, Budi Tjahjono\*, **SAS (Sino-American Silicon Products Inc.)**  
 Adam Hsu, **Shuo-Hsien, LinYang PV**  
 Marco Huber, Dirk Scholze, Peter Wohlfart, Zhenao Zhang, **Singulus Technologies**  
 Armin Aberle, **Solar Energy Research Institute of Singapore**  
 Dirk Holger Neuhaus, Phedon Palinginis, Christian Koch, **SolarWorld Industries GmbH**  
 Ingvar Åberg, Arno Stassen, **Sol Voltaics**  
 Peter Wolf, **Suzhou Maxwell Automation Equipment**  
 Paul Ni\*, **Suzhou Talesun Solar Technologies Co., Ltd**  
 Sven Kramer, **teamtechnik**

Grigory Demenik, **Technology K**  
Bram Hoex, **University of New South Wales**  
Norbert Lenck, Axel Metz\*, **VDE Renewables**  
Jutta Trube\*, **VDMA**  
Ivan Saha\*, **Vikram Solar**  
Richard Moreth, **Vitronic**  
Kristin Luedemann, **VON ARDENNE GmbH**  
Erich Dornberger, **Wacker Chemie AG**  
Rulong Chen\*, Haohao Zhou, **Wuxi Suntech Power Co., Ltd**  
Gang Yu, **Zhenjiang Rietech New Energy Science Technology Co., Ltd**

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\*Steering committee of the ITRPV, consisting of Co-chairs and Coordinator

## 9.2. Image Source

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**VDMA**

Photovoltaic Equipment

Lyoner Str. 18  
60528 Frankfurt am Main  
Germany

**Contact**

Dr. Jutta Trube

Phone +49 69 6603 1897

E-Mail [jutta.trube@vdma.org](mailto:jutta.trube@vdma.org)

Internet [www.itrpv.org](http://www.itrpv.org)

[www.itrpv.org](http://www.itrpv.org)